μPD168807

4-ch Output DC-DC Converter Controller IC

R03DS0001EJ0200
Rev.2.00
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Description

The μPD168807 is a DC-DC converter controller IC that consists of 3-ch output circuits containing power MOSFET and 1-ch output circuits that can directly drive power MOSFET.

Features

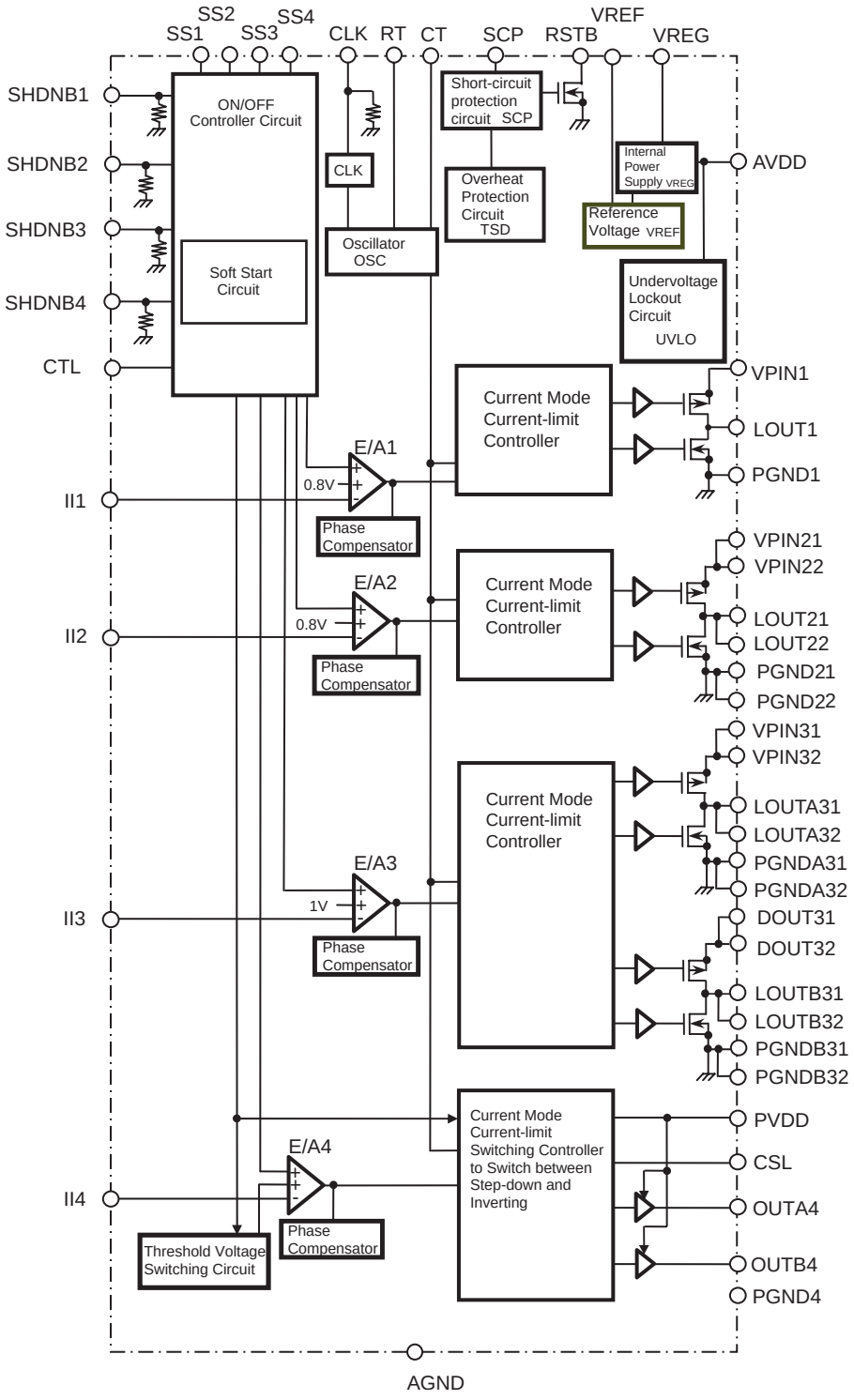
- Uses a synchronous rectification type step-down circuit (ch1, ch2)
- Uses a synchronous rectification type step-up/down circuit (ch3)
- Uses a switching circuit to switch between step-down (using synchronous rectification) and inverting (using asynchronous rectification) (ch4)
- Incorporates a power MOSFET (ch1 to ch3)
- Incorporates a phase compensator (ch1 to ch4)
- Operating frequency: 300 kHz to 1500 kHz
- Can use an external clock (to improve the oscillating frequency accuracy)
- Incorporates a timer-latch-type short-circuit protector
- Incorporates a timer-latch-type overheat protector (shutdown temperature: 150ºC or higher)
- Incorporates a recovery-type undervoltage lockout circuit
- Housed in a 48-pin VQFN package

Ordering Information

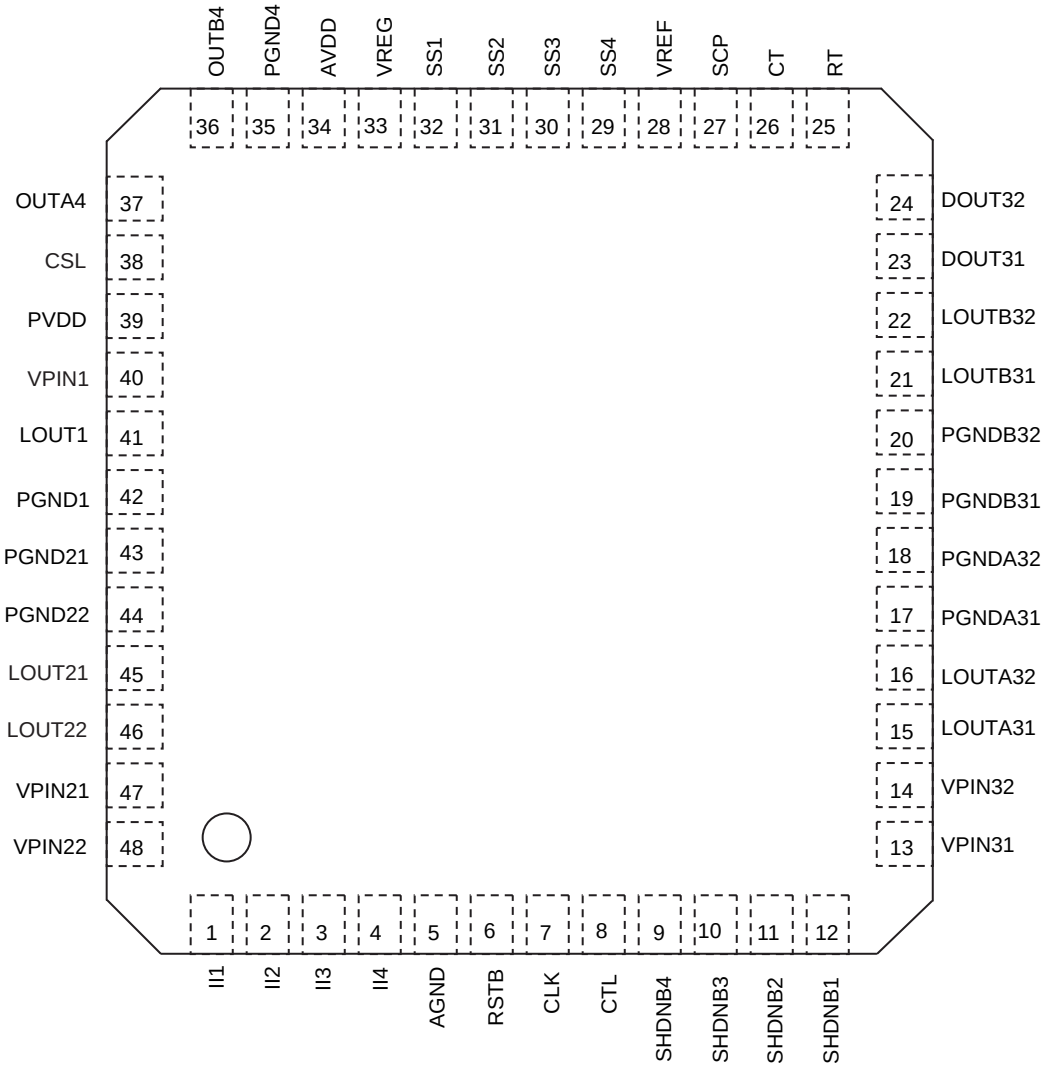
Part No.	Package	Packing style
μPD168807K9-4EG-E1-A	48-pin plastic VQFN	Embossed taping

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

1. Block Diagram



2. Pin Configuration (Top View)



3. Pin Function

Pin No.	Symbol	I/O	Function
1	II1	Input	Inverted input for error amplifier of ch1
2	II2	Input	Inverted input for error amplifier of ch2
3	II3	Input	Inverted input for error amplifier of ch3
4	II4	Input	Inverted input for error amplifier of ch4
5	AGND	Ground	Analog ground
6	RSTB	Output	Short-circuit detection signal pin (open-drain output)
7	CLK	Input	Clock signal Input
8	CTL	Input	Step-down circuit / inverting circuit operation setting mode of ch4
9	SHDNB4	Input	Output ON/OFF of ch4
10	SHDNB3	Input	Output ON/OFF of ch3
11	SHDNB2	Input	Output ON/OFF of ch2
12	SHDNB1	Input	Output ON/OFF of ch1
13	VPIN31	Power Supply	Output stage power input 1 of ch3
14	VPIN32	Power Supply	Output stage power input 2 of ch3
15	LOUTA31	Output	Inductor connection 1 for ch3A
16	LOUTA32	Output	Inductor connection 2 for ch3A
17	PGNDA31	Ground	Power ground
18	PGNDA32	Ground	Power ground
19	PGNDB31	Ground	Power ground
20	PGNDB32	Ground	Power ground
21	LOUTB31	Output	Inductor connection 1 for ch3B
22	LOUTB32	Output	Inductor connection 2 for ch3B
23	DOUT31	Output	Output 1 of ch3
24	DOUT32	Output	Output 2 of ch3
25	RT	–	Resistance connection for triangular wave generation
26	CT	–	Capacitor connection for triangular wave generation
27	SCP	–	Capacitor connection pin for timer latch
28	VREF	Output	Reference voltage output
29	SS4	–	Capacitor connection for soft start of ch4
30	SS3	–	Capacitor connection for soft start of ch3
31	SS2	–	Capacitor connection for soft start of ch2
32	SS1	–	Capacitor connection for soft start of ch1
33	VREG	Output	Internal power supply output
34	AVDD	Power Supply	Analog block power supply
35	PGND4	Ground	Power ground
36	OUTB4	Output	Output of ch4B
37	OUTA4	Output	Output of ch4A
38	CSL	Input	Load current detection of ch4 (Low-voltage side)
39	PVDD	Power Supply and Input	Power supply for output buffer stage, load current detection of ch4 (high-voltage side)
40	VPIN1	Power Supply	Output stage power input of ch1
41	LOUT1	Output	Inductor connection for ch1
42	PGND1	Ground	Power ground
43	PGND21	Ground	Power ground
44	PGND22	Ground	Power ground
45	LOUT21	Output	Inductor connection 1 for ch2
46	LOUT22	Output	Inductor connection 2 for ch2
47	VPIN21	Power Supply	Output stage power input 1 of ch2
48	VPIN22	Power Supply	Output stage power input 2 of ch2

4. Electrical Specifications

Absolute Maximum Ratings

(Unless otherwise specified, T_A = 25°C, glass epoxy four layer substrate, 100 mm x 100 mm x 1.0 mmt, Copper film: 50%)

Parameter	Symbol	Condition	Parameter	Unit
Analog power supply voltage (AVDD pin)	AV_{DD}		–0.5 to +15	V
Buffer stage power supply voltage (PVDD pin)	PV_{DD}		–0.5 to +15	V
CSL pin applied voltage	V_{CSL}	CSL	–0.5 to +15	V
VPIN pin applied voltage	V_{PIN}	VPIN1 to VPIN32	–0.5 to +15	V
II pin applied voltage	V_{II}	II1 to II4	–0.5 to +4.0	V
SHDNB pin applied voltage	V_{SHDNB}	SHDNB1 to SHDNB4	–0.5 to +15	V
CTL pin applied voltage	V_{CTL}	CTL	–0.5 to +15	V
CLK pin applied voltage	V_{CLK}	CLK	–0.5 to +15	V
RSTB pin applied voltage	V_{RSTB}	RSTB	–0.5 to +15	V
VPIN1 pin sink current (DC)	$I_{PIN1(DC)-}$		1200	mA
VPIN1 pin sink current (pulse)	$I_{PIN1(pulse)-}$		1600	mA
VPIN21 + VPIN22 pin sink current (DC)	$I_{PIN2(DC)-}$	VPIN21 + VPIN22	1500	mA
VPIN21 + VPIN22 sink current (pulse)	$I_{PIN2(pulse)-}$	VPIN21 + VPIN22	1900	mA
VPIN31 + VPIN32 pin sink current (DC)	$I_{PIN3(DC)-}$	VPIN31 + VPIN32	1200	mA
VPIN31 + VPIN32 sink current (pulse)	$I_{PIN3\ (pulse)-}$	VPIN31 + VPIN32	1600	mA
LOUT1 output source current (DC)	$I_{LO1(DC)+}$		1200	mA
LOUT1 output source current (pulse)	$I_{LO1(pulse)+}$		1600	mA
LOUT21 + LOUT22 output source current (DC)	$I_{LO2(DC)+}$	LOUT21 + LOUT22	1500	mA
LOUT21 + LOUT22 output source current (pulse)	$I_{LO2(pulse)+}$	LOUT21 + LOUT22	1900	mA
LOUTA31 + LOUTA32, DOUT31 + DOUT32 output source current (DC)	$I_{LOA3,\ DO3(DC)+}$	LOUTA31 + LOUTA32 DOUT31 + DOUT32	1200	mA
LOUTA31 + LOUTA32, DOUT31 + DOUT32 output source current (pulse)	$I_{LOA3,\ DO3\ (pulse)+}$	LOUTA31 + LOUTA32 DOUT31 + DOUT32	1600	mA
LOUTB31 + LOUTB32 output sink current (DC)	$I_{LOB3(DC)-}$	LOUTB31 + LOUTB32	1200	mA
LOUTB31 + LOUTB32 output sink current (pulse)	$I_{LOB3(pulse)-}$	LOUTB31 + LOUTB32	1600	mA
OUTA4, OUTB4 output source current (DC)	$I_{OA4,\ B4(DC)+}$		30	mA
OUTA4, OUTB4 output source current (pulse)	$I_{OA4,\ B4(pulse)+}$		400	mA
OUTA4, OUTB4 output sink current (DC)	$I_{OA4,\ B4(DC)-}$		30	mA
OUTA4, OUTB4 output sink current (pulse)	$I_{OA4,\ B4(pulse)-}$		400	mA
Total power dissipation	P_T	$T_A \le$ +25°C	1700[*1]	mW
Operating ambient temperature	T_A		–20 to +85	°C
Operating junction temperature	T_J		–20 to +150	°C
Storage temperature	T_{stg}		–55 to +150	°C

Note: [*]1. This is the value at $T_A \le$ +25°C. Where $T_A >$ +25°C, perform derating at −13.6 mW/°C.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

(Unless otherwise specified, T_A = 25°C, glass epoxy four layer substrate, 100 mm x 100 mm x 1.0 mmt, Copper film: 50%)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analog power supply voltage (AVDD pin)	AV_{DD}		4.0	7.4	14.5	V
Buffer stage power supply voltage (PVDD pin)	PV_{DD}			AV_{DD}		V
CSL pin applied voltage	V_{CSL}	CSL		AV_{DD}		V
VPIN pin applied voltage	V_{PIN}	VPIN1 to VPIN32	4.0	7.4	14.5	V
II pin applied voltage	V_{II}	II1 to II4	0		V_{REG}	V
SHDNB pin applied voltage	V_{SHDNB}	SHDNB1 to SHDNB4	0		AV_{DD}	V
CTL pin applied voltage	V_{CTL}	CTL	0		AV_{DD}	V
CLK pin applied voltage	V_{CLK}	CLK	0		AV_{DD}	V
RSTB pin applied voltage	V_{RSTB}	RSTB	0		AV_{DD}	V
CLK input frequency	f_{CLK}	CLK	300	750	1500	kHz
Oscillation frequency	f_{OSC}		300	750	1500	kHz
Oscillator timing resistance	R_T	RT		1.2		kΩ
Oscillator timing capacitance	C_T	CT		220		pF
Soft start capacitance	C_{SS}	SS1 to SS4		0.01		μF
SCP pin capacitor capacitance	C_{SCP}	SCP		0.1		μF
VREF pin capacitor capacitance	C_{REF}	V_{REF}		0.1		μF
VREG pin capacitor capacitance	C_{REG}	V_{REG}		1.0		μF

Electrical Specifications

(Unless otherwise specified, T_A = 25°C, AV_{DD} = PV_{DD} = $V_{PIN1\ to\ 32}$ = DOUT31 to 32 = 7.4 V, f_{OSC} = 750 kHz)

Total						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Standby current	$I_{DD(SHDN)}$	AI_{DD}+PI_{DD}+IP_{IN1}+IP_{IN21}+IP_{IN22}+IP_{IN31}+IP_{IN32} SHDNB1 to SHDNB4 = AGND		1	3	μA
Circuit operation current 1	AI_{DD}	AI_{DD}, CTL= AV_{DD} (at ch4 inverting) ch1 to ch4 = "ON", II1 = II2 = II3 = V_{REG} II4 = AGND		4	8	mA
Circuit operation current 2	PI_{DD}	PI_{DD}, CTL = AV_{DD} (at ch4 inverting) ch1 to ch4 = "ON", II1 = II2 = II3 = II4 = V_{REG}, no load		4	8	mA
Reference voltage block						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Reference voltage	V_{REF}	I_{REF} = 0 mA	1.98	2.00	2.02	V
Input regulation	$V_{REF(REGIN)}$	AV_{DD} = PV_{DD} = 4.0 V to 14.5 V		10	20	mV
Load regulation	$V_{REF(REGL)}$	I_{REF} = 0 to 1.0 mA		20	40	mV
Temperature characteristic				0.5		%
Internal power supply block						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Internal power supply voltage	V_{REG}	I_{REG} = 0 mA	3.0	3.3	3.6	V
Low-voltage malfunctioning prevention circuit						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Operation start voltage during rise time	$AV_{DD(L-H)}$	AVDD pin voltage detected	2.50	3.15	3.80	V
Operation stop voltage	$AV_{DD(H-L)}$	AVDD pin voltage detected	2.30	2.95	3.60	V
Short-circuit protection circuit						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
II1 input detection voltage (ch1)	$V_{TH(II)1}$	II1 pin	0.5	0.6	0.7	V
II2 input detection voltage (ch2)	$V_{TH(II)2}$	II2 pin	0.5	0.6	0.7	V
II3 input detection voltage (ch3)	$V_{TH(II)3}$	II3 pin	0.7	0.8	0.9	V
II4 input detection voltage 1 (ch4 step-down)	$V_{TH(II)41}$	II4 pin, when step-down	0.5	0.6	0.7	V
II4 input detection voltage 2 (ch4 inverting)	$V_{TH(II)42}$	II4 pin, when inverting	0.5	0.6	0.7	V
DLY detection voltage	$V_{TH(DLY)}$	SCP pin	0.6	0.9	1.2	V
Short-circuit source current	I_{OUT}		0.60	0.85	1.20	μA
RSTB pin output voltage	V_{RSTB}	I_{RSTB-} = 0.1 mA			0.1	V
RSTB pin leakage voltage	$I_{LEAK-RSTB}$	SHDNB1 to SHDNB4 = AGND			1	μA
Oscillation block						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Low-level threshold voltage	$V_{TH(L)}$		0.3	0.4	0.5	V
High-level threshold voltage	$V_{TH(H)}$		0.7	0.8	0.9	V
Frequency setting accuracy	f_{OSC}	C_T = 220 pF, R_T = 1.2 kΩ	–10		+10	%
Input stability	Δf_{OSC}	AV_{DD} = PV_{DD} = 4.0 V to 14.5 V	–3		+3	%

Electrical Specifications

(Unless otherwise specified, T_A = 25°C, AV_{DD} = PV_{DD} = $V_{PIN1\ to\ 32}$ = DOUT31 to 32 = 7.4 V, f_{OSC} = 750 kHz)

Soft start block						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Charging current	I_{SS1}	SS1 to SS4 = 0 V, ch4 (when step-down)	2.8	4.0	5.6	μA
Discharging current	I_{SS2}	SS4 = 2 V, ch4 (when inverting)	2.8	4.0	5.6	μA
PWM block						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Maximum duty 1	$D_{MAX.1}$	ch1, ch2, ch3 step-down, ch4 step-down		100		%
Maximum duty 2	$D_{MAX.2}$	ch3 step-up, ch4 inverting		85		%
E/A block (ch1 to ch7)						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
E/A 1 input threshold voltage	V_{ITH1}	Including input offset	0.78	0.80	0.82	V
E/A 2 input threshold voltage	V_{ITH2}	Including input offset	0.78	0.80	0.82	V
E/A 3 input threshold voltage	V_{ITH3}	Including input offset	0.98	1.00	1.02	V
E/A 4 input threshold voltage 1	V_{ITH4-1}	Including input offset, when step-down	0.78	0.80	0.82	V
E/A 4 input threshold voltage 2	V_{ITH4-2}	Including input offset, when inverting	0.38	0.40	0.42	V
Output block (ch1)						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
P-ch output ON resistance	R_{on-p1}	I_O = 100 mA		0.40	0.60	Ω
N-ch output ON resistance	R_{on-n1}	I_O = –100 mA		0.30	0.50	Ω
Output block (ch2)						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
P-ch output ON resistance	R_{on-p2}	I_O = 100 mA		0.35	0.55	Ω
N-ch output ON resistance	R_{on-n2}	I_O = –100 mA		0.25	0.40	Ω
Output block (ch3)						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
P-ch output ON resistance	R_{on-p3}	I_O = 100 mA		0.25	0.40	Ω
N-ch output ON resistance	R_{on-n3}	I_O = –100 mA		0.25	0.40	Ω
Output block (ch4)						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
P-ch output ON resistance	R_{on-p4}	I_O = 20 mA		30	60	Ω
N-ch output ON resistance	R_{on-n4}	I_O = –20 mA		10	20	Ω
ON/OFF controller block						
Parameter	**Symbol**	**Condition**	**MIN.**	**TYP.**	**MAX.**	**Unit**
Threshold voltage	$V_{TH(SHDNB)}$	SHDNB1 to SHDNB4, CTL, CLK	0.8		2.0	V
Input pull-down resistance	R_{IND}	SHDNB1 to SHDNB4, CLK	200	400	700	kΩ

5. Output Control Block

• CTL: ch4 Operation setting mode

Signal	ch4 step-down circuit / inverting circuit operation setting
L	Step-down
H	Inverting

Remark L: Low level, H: High level

Caution Fix the CTL pin during at circuit operation.
The pull-down resistor is not connected with the CTL pin. Be sure to externally fix the pin to L or H.

• SHDNB1 to SHDNB4: ON/OFF Setting Mode

SHDNB1	SHDNB2	SHDNB3	SHDNB4	Common Circuit	ch1	ch2	ch3	ch4
L	L	L	L	OFF	OFF	OFF	OFF	OFF
H	L	L	L	ON	ON	OFF	OFF	OFF
L	H	L	L	ON	OFF	ON	OFF	OFF
L	L	H	L	ON	OFF	OFF	ON	OFF
L	L	L	H	ON	OFF	OFF	OFF	ON
H	H	H	H	ON	ON	ON	ON	ON

Remark L: Low level, H: High level
Common Circuit: Reference voltage block, internal power supply block, oscillator block and so forth
OFF: circuit stand-by, ON: circuit operation status

• ch1 to ch4 output mode

SHDNB1 to SHDNB4	VREG	VREF	ch1	ch2	ch3			ch4			
								(Step-down CTL = L)		(Inverting CTL = H)	
			LOUT1	LOUT21 LOUT22	LOUTA31 LOUTA32	LOUTB31 LOUTB32	DOUT31 DOUT32	OUTA4	OUTB4	OUTA4	OUTB4
L	AGND	AGND	HiZ					PVDD	PGND	PVDD	PGND
H	V_{REG}	V_{REF}	V_{PIN1} or PGND	$V_{PIN21,22}$ or PGND	$V_{PIN31,32}$ or PGND	V_{OUT3} or PGND	V_{OUT3}	PVDD or PGND	PVDD or PGND	PVDD or PGND	PGND

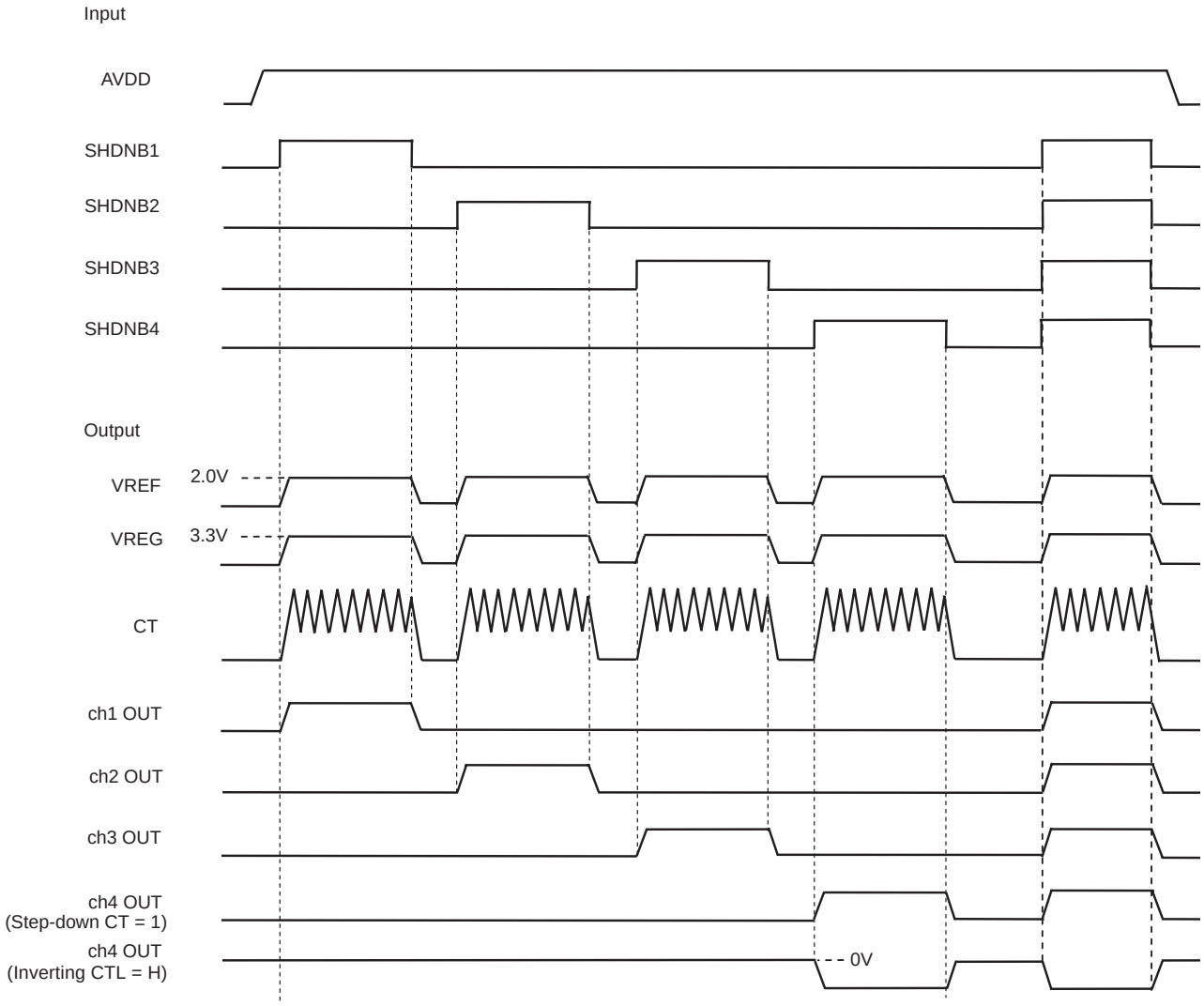
Remark L: Low level, H: High level, HiZ: High impedance
V_{OUT3}: ch3 output voltage

• RSTB: Circuit Protection operation identification mode

IC Operation Status	RSTB Output Status
Stand-by and normal operation	HiZ
Short-circuit protection operation and overheat protection operation (All channel are latched to OFF.)	L

Remark L: Low level, HiZ: High impedance

6. Timing Chart



7. Operation of Each Block (Overview)

Reference Voltage Block

The reference voltage block outputs a reference voltage (2.0 V TYP) that has been temperature-compensated by the voltage supplied from the internal power supply block (3.3 V TYP). This reference voltage is used as the reference voltage for all the internal circuits and a current of up to 1 mA can be output to an external circuit from the VREF pin (pin 28).

Internal power supply block

The internal power supply block generates 3.3 V (TYP.) from analog power supply through AVDD pin (34 pin). This block provides internal circuits with electric sources; however, not supposed to be used externally.

Oscillator block

The oscillator block spontaneously oscillates when a timing capacitance and a timing resistance are respectively connected to the CT pin (pin 26) and RT pin (pin 25), and outputs a symmetrical triangular wave with an amplitude of 0.4 to 0.8 V (TYP.) to the CT pin.

E/A block (error amplifier)

The circuit configuration of all error amplifiers E/A1, E/A2, E/A3 and E/A4 is identical. All E/As have an internal phase compensator. Pin II inputs an inverted signal to the E/A block. The input threshold voltages of the E/A block are about 0.8 V for E/A1, E/A2 and E/A4 (CTL = L, when step-down), 1.0 V (TYP.) for E/A3 and 0.4 V (TYP.) for E/A4 (CTL = H, when inverting).

Output control block

The output control block controls the output ON duty by using the E/A output signal and the signal output from the current detection amplifier. The maximum duty is 100% (TYP) when ch1 and ch2 operate, and ch3 (step-down) and ch4 (step-down, CTL = L) operate, and 85% (TYP) when ch3 (step-up) operates and ch4 operates as the inverting circuit (CTL = H).

Output circuit block

The output circuit block of ch1 to ch3 includes a power MOSFET. The output current capacity of ch1 is 1.6 A (MAX) when a switching pulse is output and 1.2 A (MAX) when DC is output. The output current capacity of ch2 is 1.9 A (MAX) when a switching pulse is output and 1.5 A (MAX) when DC is output. The output current capacity of ch3 is 1.6 A (MAX) when a switching pulse is output and 1.2 A (MAX) when DC is output. The output circuit block of ch4 has a push-pull configuration and can directly drive the power MOSFET. The output current capacity of ch4 is 400 mA (MAX) when a pulse is output and 30 mA (MAX) when DC is output.

ON/OFF control block

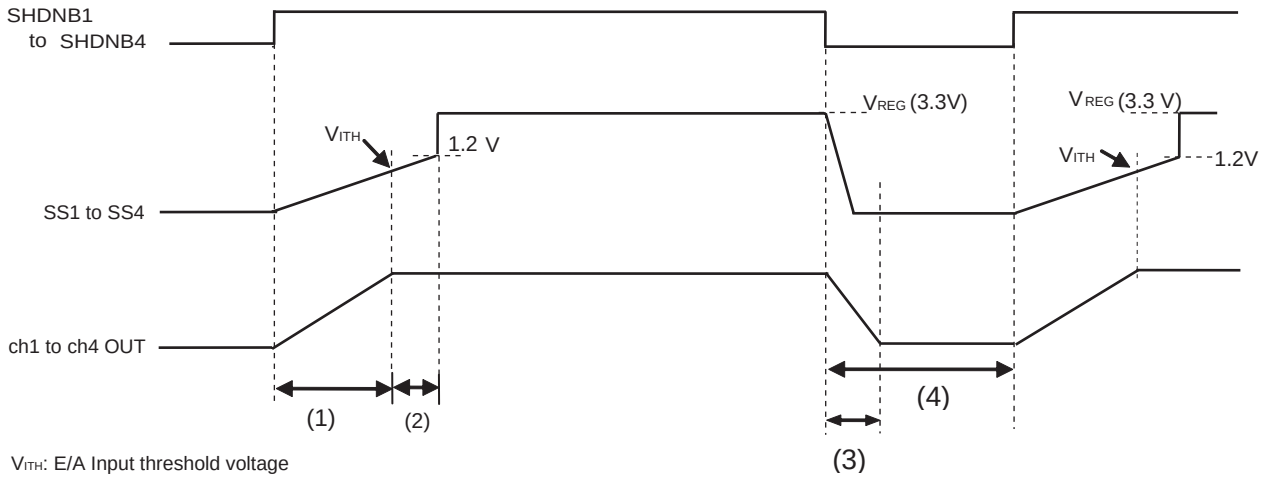
This circuit can turn on/off the output voltage of each channel by using the SHDNB1 pin to SHDNB4 pin and an external signal. When the SHDNB1 to SHDNB4 pins are made low, a shut-down circuit operates, shutting down the output of each channel. When the SHDNB1 to SHDNB4 pins are made high, the shut-down circuit stops, ch1 to ch4 are soft-started and their output voltage rises.

Soft start circuit block

(1) Soft start operation when ch1 to ch3 start and ch4 (step-down, CTL = L) start

A soft start is triggered by charging the capacitors connected to the SS1 to SS4 pins and slowly increasing the E/A threshold voltage level. When a soft start is triggered, the SS pin voltage is connected to the E/A non-inverted input and the E/A non-inverted input voltage rises from 0 V. The output ON duty then slowly increases, executing the soft start.

Timing chart (when ch1 to ch3 start and ch4 (step-down, CTL = L) start



<1> Soft start triggered

- When the level of the SHDNB pin for each channel is changed from low to high, the external soft start capacitors for each channel (connected to the SS pins) start charging and voltage output begins.
- Charge current for external soft start capacitors = 4 μA (TYP)

<2> End of soft start

- When the voltage of each channel's SS pin reaches the E/A input threshold voltage level, the soft start of each channel ends.
- Even after the soft start ends, the SS pin voltage continues to rise until it reaches at least 1.2 V, at which point the SS pin voltage is pulled up to VREG (3.3 V).

<3> Stopping output

- When the level of the SHDNB pin for each channel is changed from high to low, output from each channel stops and the external soft start capacitors discharge.

<4> Resuming output

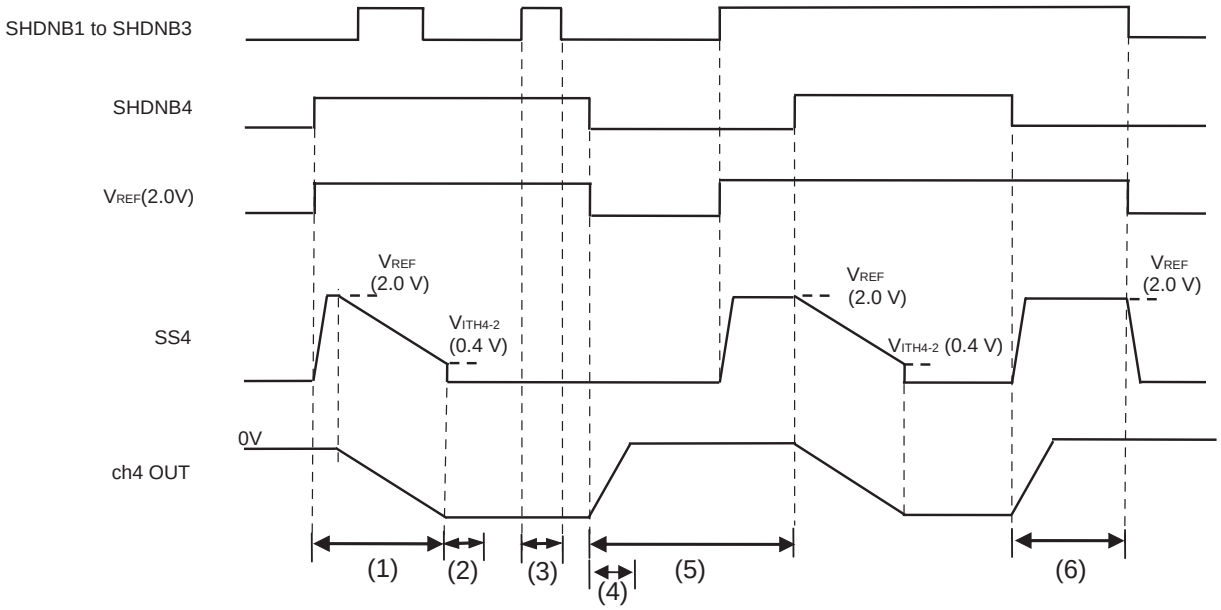
- After output has been stopped (after the SHDNB pin level has been changed from high to low), it takes at least 100 μs before output can be restarted.

Caution: This IC does not include an output capacitor discharge circuit. Therefore, be careful about the output capacitor discharge time.

(2) Soft start operation when ch4 is operating as the inverting circuit (CTL = H)

A soft start of the inverting circuit is triggered by discharging the capacitor connected to the SS4 pin and slowly decreasing the E/A4 threshold voltage level. The capacitor connected to the SS4 pin charges rapidly by means of the reference voltage V_{REF} (2 V) when the level of any of the SHDNB1 to 4 pins is changed from low to high while ch4 is not operating. When a soft start is triggered, the SS4 pin voltage is connected to the E/A4 non-inverted input and the E/A4 non-inverted input voltage falls from 2 V. The output ON duty then slowly increases, executing the soft start.

Timing chart (when ch4 is operating as the inverting circuit (CTL = H))



V_{ITH4-2}: E/A4 input threshold voltage (when inverting)

<1> Soft start triggered

- When the level of any of the SHDNB1 to 4 pins is changed from low to high while the circuit is on standby (all channels are stopped), the external soft start capacitor (connected to the SS4 pin) starts charging.
- After the external soft start capacitor is finished charging, if the level of the SHDNB4 pin is high, the external soft start capacitor starts discharging and ch4 output starts.
- Discharge current for external soft start capacitors = 4 μA (TYP)
- After the level of the SHDNB4 pin has changed from low to high while the circuit is on standby (all channels are stopped), the time between the start of charging and the start of discharging depends on the circuit conditions (but is no more than 100 μs).

<2> End of soft start

- When the voltage of the SS4 pin falls to the E/A4 input threshold voltage level (0.4 V TYP), ch4 ends the startup.
- Once the voltage of the SS4 pin reaches 0.4 V, the SS4 pin voltage is pulled down to ground level.

<3> While ch4 is operating

- Even if the level of any of the SHDNB1 to 3 pins is changed from low to high, if ch4 is operating, the soft start capacitor connected to the SS4 pin is not charged and the SS4 pin voltage remains at the GND level.

<4> Stopping output

- When the level of the SHDNB4 pin is changed from high to low, ch4 output stops.

<5> Resuming output

- After the SHDNB4 pin level has been changed from high to low, it takes at least 100 μs (provisional value) before output can be restarted.

<6> When ch4 operation is stopped

- If the level of any of the SHDNB1 to 3 pins is high while ch4 is stopped (by changing the level of the SHDNB4 pin from high to low), the external soft start capacitor starts charging.
- Once the capacitor has finished charging and all the SHDNB pins are low level, the external soft start capacitor will discharge.

Caution: This IC does not include an output capacitor discharge circuit. Therefore, be careful about the output capacitor discharge time.

External clock

The IC can be run on a clock frequency by inputting a clock pulse to the CLK pin (pin 7). The accuracy of the oscillating frequency at this time will depend on the accuracy of the clock frequency.

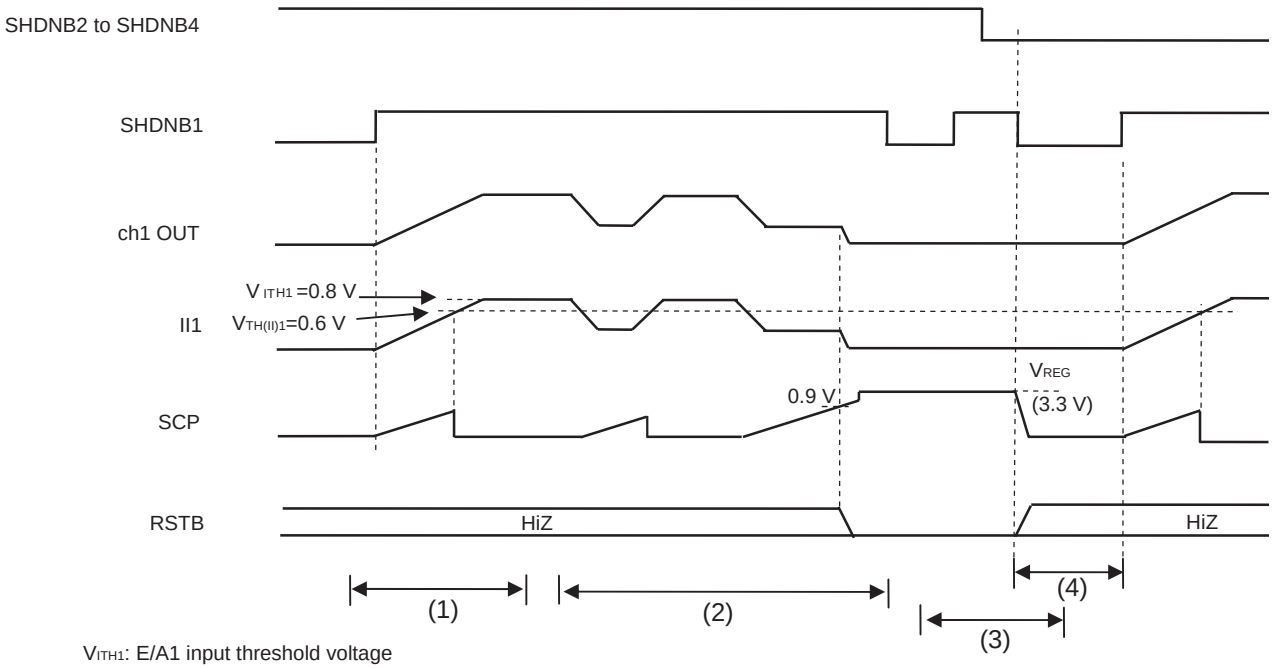
Short-circuit protection circuit (Timer latch type)

When the voltage of ch1 to ch3 and ch4 operating as a step-down circuit (CTL = L) drops (or when the voltage of ch4 rises if ch4 is operating as inverting circuit), the voltage of the E/A inverted input pin to which the output is being fed back also drops (or rises in the case of ch4 if ch4 is operating as inverting circuit). If this inverted input pin voltage falls below the input detection voltage of the short-circuit protection circuit (E/A1 = VTH1 = 0.6 V, E/A2 = VTH2 = 0.6 V, E/A3 = VTH3 = 0.8 V, E/A4 = VTH4 = 0.6 V) (or rises above the input detection voltage (E/A4 = VTH4 = 0.6 V) if ch4 is operating as inverting circuit), the timer circuit starts operating and the capacitor connected to the SCP pin (pin 27) (CSCP) starts charging. When the voltage of the capacitor connected to the SCP pin reaches 0.9 V (TYP), all the outputs of the IC are latched to OFF. At this time, the level of the RSTB pin (pin 6) is GND.

As long as the voltage of any of the E/A inverted input pins of ch1 to ch4 is below the input detection voltage of the short-circuit protection circuit (or is above the input detection voltage if ch4 is operating as inverting circuit), the capacitor connected to the SCP pin continues charging.

When the short-circuit protection circuit is operating, to reset the latch circuit, either drop the level of the power supply voltage (AV_{DD}) to GND or change the level of all the SHDNB1 to SHDNB4 pins from high to low. After the latch status is reset, it takes at least 100 μs before output can be restarted.

Timing chart (when ch1 is short circuited)



V_{ITH1}: E/A1 input threshold voltage
$V_{TH(II)}$: Short-curcuit protection circuit II1 input detection voltage

<1> Soft start triggered

- The soft start operation is asynchronous to the short-circuit protection operation.

<2> Short-circuit protection operation

- After a short circuit has been detected (when the SCP pin voltage rises to 0.9 V), output from all channels stops (the outputs are latched to OFF).
  Common circuits (such as the reference voltage block, internal power supply block, and oscillator) continue operating.
- The short detection pin (RSTB) operates when the short-circuit protection circuit operates.
  During normal operation: high impedance; when the short-circuit protection circuit is operating: low level

<3> Cancelling short-circuit protection

- The latch status is reset when the level of all the SHDNB pins is changed from high to low.

<4> Resuming output

- After the latch status is reset, it takes at least 100 μs before output can be restarted.

Overheat protection circuit (timer latch type)

After overheating has been detected (shutdown temperature: 150ºC or higher), output from all channels stops (the outputs are latched to OFF). Common circuits (such as the reference voltage block, internal power supply block, and oscillator) continue operating.

When the overheat protection circuit is operating, to reset the latch circuit, either drop the level of the power supply voltage (AV_{DD}) to GND or change the level of all the SHDNB1 to SHDNB4 pins from high to low. After the latch status is reset, it takes at least 100 us before output can be restarted.

Undervoltage lockout circuit (auto recovery type)

If an undervoltage is detected (if the power supply voltage (AV_{DD}) is too low), output from all channels and common circuits (such as the reference voltage block, internal power supply block, and oscillator) stop and the IC is put on standby.

Once the AV_{DD} voltage is recovered, output automatically resumes. While the undervoltage lockout circuit is operating, the output voltage will not recover even if the SHDNB pins are manipulated (the IC remains on standby).

Current limiting

If an overcurrent occurs, the current is limited on a pulse-by-pulse basis. If the current sensor detects an overcurrent, the current is limited and the switching operation of the PoMOS in the output stage stops until the next cycle.

When the current is limited, the output voltage of the channel on which the overcurrent occurred drops. If the II pin voltage falls below the II input detection voltage (or rises above the II input detection voltage in the case of ch4 if ch4 is operating as inverting circuit), the short-circuit protection circuit starts operating.

8. Advance on Designing

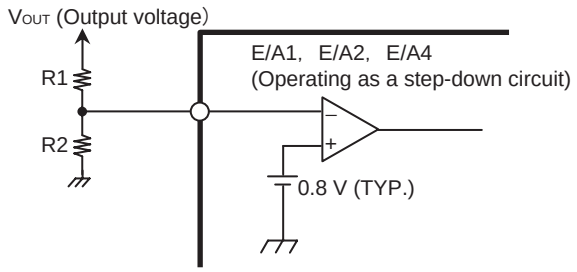
Setting Output Voltage

The output voltage settings are shown in the figures below. The output voltage can be calculated by using the equations shown in these figures.

The input threshold voltage of the error amplifier is 0.8 V (TYP) for E/A1, E/A2, and E/A4 when ch4 is operating as a step-down circuit, and 1.0 V (TYP) for E/A3 and 0.4 V (TYP) for E/A4 when ch4 is operating as inverting circuit.

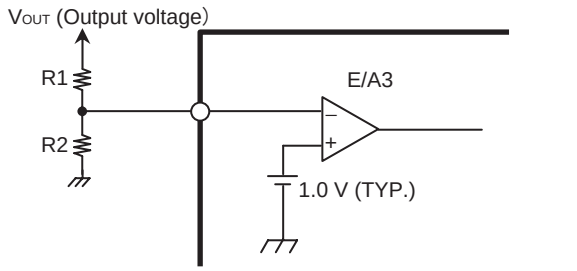
Setting output voltage of ch1, ch2, and ch4 (operating as a step-down circuit)

$V_{OUT} = (1+R1/R2) \times 0.8$



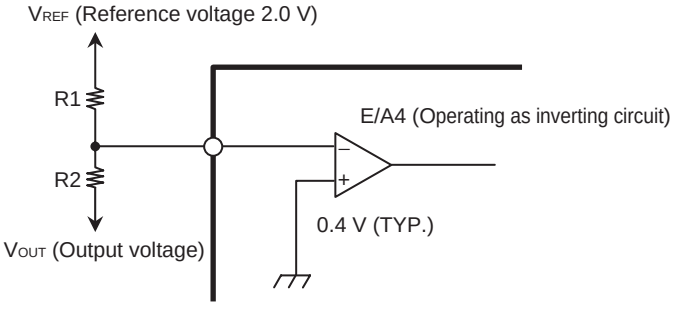
Setting output voltage of ch3

$V_{OUT} = (1+R1/R2) \times 1.0$



Setting output voltage of ch4 (operating as inverting circuit)

$V_{OUT} = V_{REF} - (V_{REF} - 0.4) \times (1+R2/R1)$



Setting Oscillation Frequency

The oscillation frequency can be arbitrarily set by the timing resistance connected to the RT pin and timing capacitance connected to the CT pin.

An approximate expression of the oscillation frequency (f_{OSC}) is shown below. However, because this expression is for approximation, mount the IC on the actual system and check the values of the parameters especially when the IC is used at a high frequency.

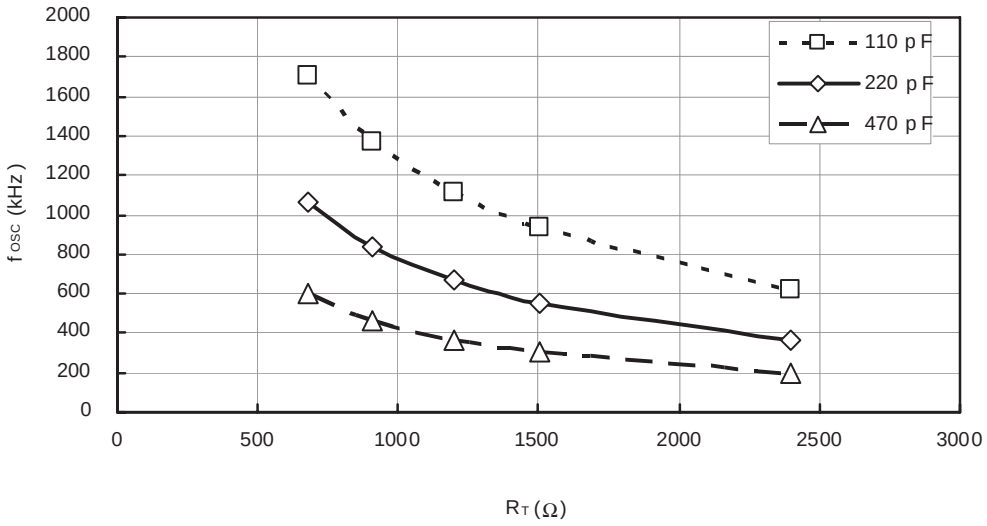
$f_{OSC} = 0.175/(C_T \times R_T)$ [Hz] (Conditions: $AV_{DD} = 7.4$ V, $T_A = 25°C$)

Example

$C_T = 220$ pF, $R_T = 1.2$ kΩ

$f_{OSC} = 0.175/(220 \times 10^{-12} \times 1200) \cong 663$ kHz

The following graph shows f_{OSC} vs. R_T characteristics with C_T as a parameter.



Calculating the soft start time

An approximate equation for calculating the soft start time (t_{SS}) is shown below.

(1) Soft start time of ch1, ch2, and ch4 when ch4 is operating as a step-down circuit:

t_{SS} [S] = 0.20 x C_{SS} [μF]

(2) Soft start time of ch3:

t_{SS} [S] = 0.25 x C_{SS} [μF]

(3) Soft start time of ch4 when ch4 is operating as inverting circuit:

t_{SS} [S] = 0.40 x C_{SS} [μF]

Calculating Delay Time of Short-circuit Protection Circuit

The following approximate expression is for calculating the delay time t_{DLY} of the short-circuit protection circuit.

t_{DLY} [s] = 1.06 x C_{SCP} [μF]

If the delay time of the short-circuit protection circuit is set to be shorter than the internally fixed soft start time, or if the load transient response of the DC-DC converter output is dull, the short-circuit protection may operate before the output voltage of a ch rises. Check the delay time of the short-circuit protection circuit by mounting the IC on an actual system.

Pin Processing When Short-circuit Protection Circuit is not used

When the short-circuit protection circuit is not used, connect the SCP pin to the AGND pin. At this time, closely monitor heating because the overheat protection circuit does not operate.

Process of I/O pin when not used

Connect the I/O pins of each ch that are not used to the pins listed below.

(Be sure to connect the pins that are necessary to the operations of power supply and GND.)

ch1 when not used

PIN NO.	Symbol	Connect pin
40	VPIN1	AVDD
41	LOUT1	OPEN
42	PGND1	PGND
1	II1	VREG
32	SS1	AGND
12	SHDNB1	OPEN or AGND

ch2 when not used

PIN NO.	Symbol	Connect pin
47	VPIN21	AVDD
48	VPIN22	AVDD
45	LOUT21	OPEN
46	LOUT22	OPEN
43	PGND21	PGND
44	PGND22	PGND
2	II2	VREG
31	SS2	AGND
11	SHDNB2	OPEN or AGND

ch3 when not used

PIN NO.	Symbol	Connect pin
13	VPIN31	AVDD
14	VPIN32	AVDD
15	LOUTA31	OPEN
16	LOUTA32	OPEN
17	PGNDA31	PGND
18	PGNDA32	PGND
21	LOUTB31	OPEN
22	LOUTB32	OPEN
23	DOUT31	PGND
24	DOUT32	PGND
19	PGNDB31	PGND
20	PGNDB32	PGND
3	II3	VREG
30	SS3	AGND
10	SHDNB3	OPEN or AGND

ch4 when not used (CTL = L)

PIN NO.	Symbol	Connect pin
37	OUTA4	PVDD
36	OUTB4	OPEN or PGND
38	CSL	PVDD
4	II4	VREG
29	SS4	AGND
9	SHDNB4	OPEN or AGND
8	CTL	AGND

Remark L: Low level

ch4 when not used (CTL = H)

PIN NO.	Symbol	Connect pin
37	OUTA4	PVDD
36	OUTB4	OPEN or PGND
38	CSL	PVDD
4	II4	AGND
29	SS4	AGND
9	SHDNB4	OPEN or AGND
8	CTL	AVDD

Remark H: High level

When external clock function is not used

PIN NO.	Symbol	Connect pin
7	CLK	OPEN or AGND

When ch4 diode rectification step-down circuit and inverting circuit operate

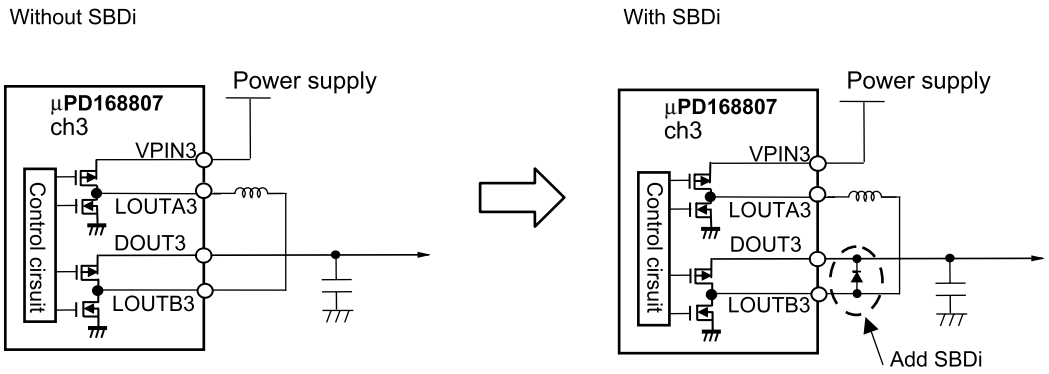
PIN NO.	Symbol	Connect pin
36	OUTB4	OPEN or PGND

When short-circuit detection signal pin (RSTB pin) is not used

PIN NO.	Symbol	Connect pin
6	RSTB	OPEN or AGND

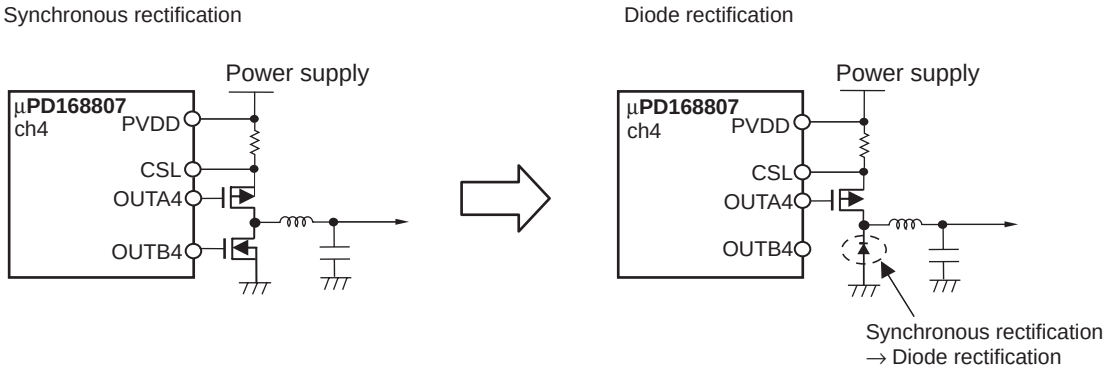
About ch3 (step-up/down circuit)

When using ch3 with an output voltage of 5.5 V or higher, operating noise as high as 60 mV (p-p) might occur. To suppress this noise, connect a Schottky barrier diode between the LOUTB3 and DOUT3 pins.



Suggestion for improving the efficiency of ch4 (step-down circuit) when the load is light

Ch4 (step-down circuit) is a synchronous rectification type step-down circuit that is used to drive an external MOSFET (Pch + Nch). However, because the load connected to ch4 is often light, ch4 can be made to operate more efficiently under a light load by changing to the diode rectification.

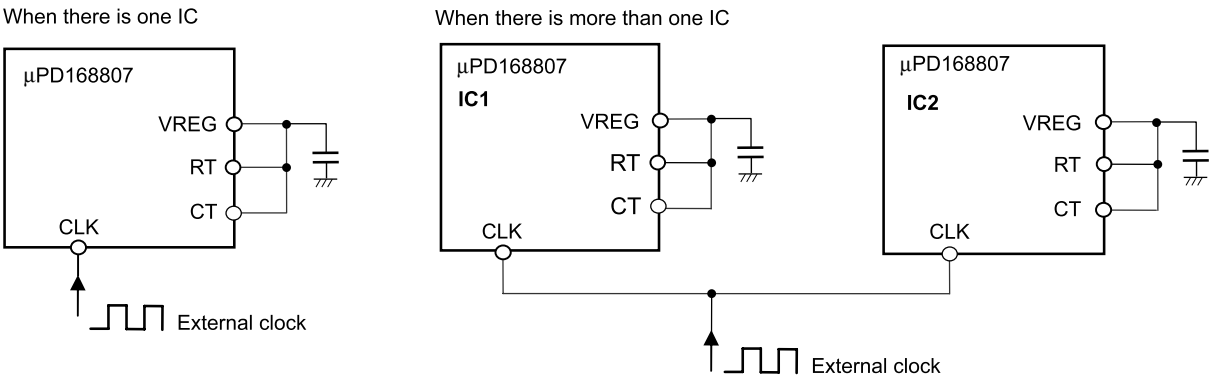


• IC pin processing during diode rectification
OUTB4: OPEN or PGND connection

External clock function

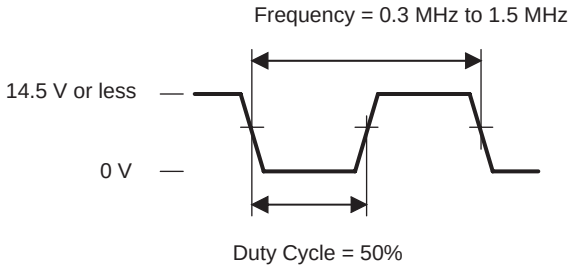
Configure the circuit as follows when using an external clock:

<R> Configure



- IC pin processing
  RT, CT: Short with VREG

External Clock Specifications



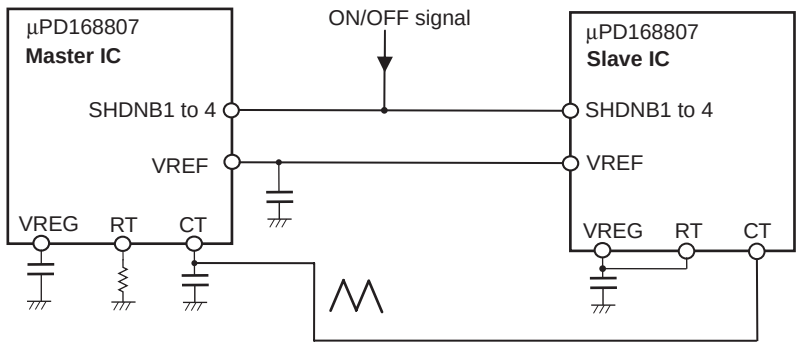
Duty cycle:	50%
Input frequency:	0.3 MHz to 1.5 MHz
Input high level voltage:	14.5 V or less
Input low level voltage:	0 V

Master-slave operation

Configure the circuit as follows when using multiple μPD168807 ICs in a master-slave configuration:

(1) Example of usual configuration

Configuration Diagram



Caution Be sure to input the signal that turns the channel started up first to the SHDNB pin of one of the channels on the slave side as well as to the SHDNB pin of the relevant channel on the master side. (The status of the VREF pin when the IC stops operating becomes AGND, so when the master IC is operating, make sure that VREF is not applied to the slave ICs that are stopped.)

- IC pin handling
  <1> Master side

  No change.

  <2> Slave side

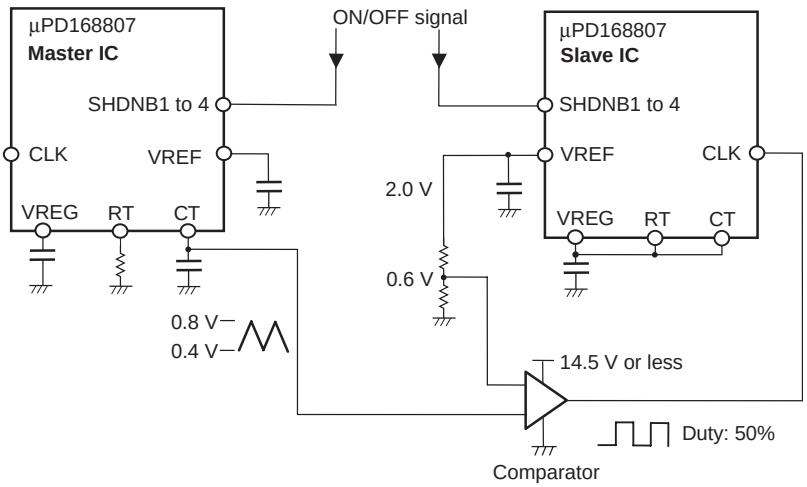
  CT: Short with CT on the master side

  RT: Short with VREG on the slave side

  VREF: Short with VREF on the master side

(2) Example of configuration when external comparator is used

Configurationi Diagram



Caution The triangular wave is 0.8 V ±0.1 V when CLK is high level and 0.4 V ±0.1 V when CLK is low level, so make sure that the 0.6 V constant voltage input to the comparator has an error of no more than ±0.1 V.

- IC pin handling
  <1> Master side

  CLK: OPEN or AGND connection

  <2> Slave side

  CT, RT: Short with VREG on the slave side

  VREF: Input the external comparator's output signal

9. Notes on Use

Prohibited mode

Always fix the CTL pin to high or low during a circuit operation.

Condition where protection circuits do not operate

When the SCP pin is connected to the AGND pin, the overheat protection circuit and short-circuit protection circuit do not operate.

Pin connection

Be sure to apply the same potential to the power supply AVDD pin and PVDD pin.

Connect all pins if there are two or more pins.

About the pull-down resistors connected to the input pins

400 kΩ (TYP) pull-down resistors are connected to the SHDNB1 to SHDNB4 pins and the CLK pin. However, in order to reduce the current consumption when the CTL pin is high level while the IC is on standby, a pull-down resistor is not connected to the CTL pin. The level of the CTL pin must therefore be fixed to either low or high externally.

Actual pattern wiring

To actually perform pattern wiring, separate the ground of the control signals from the ground of the power signals, so that these signals do not have a common impedance as much as possible. In addition, lower the high-frequency impedance by using a capacitor, so that noise is not superimposed on the VREF pin, VREG pin.

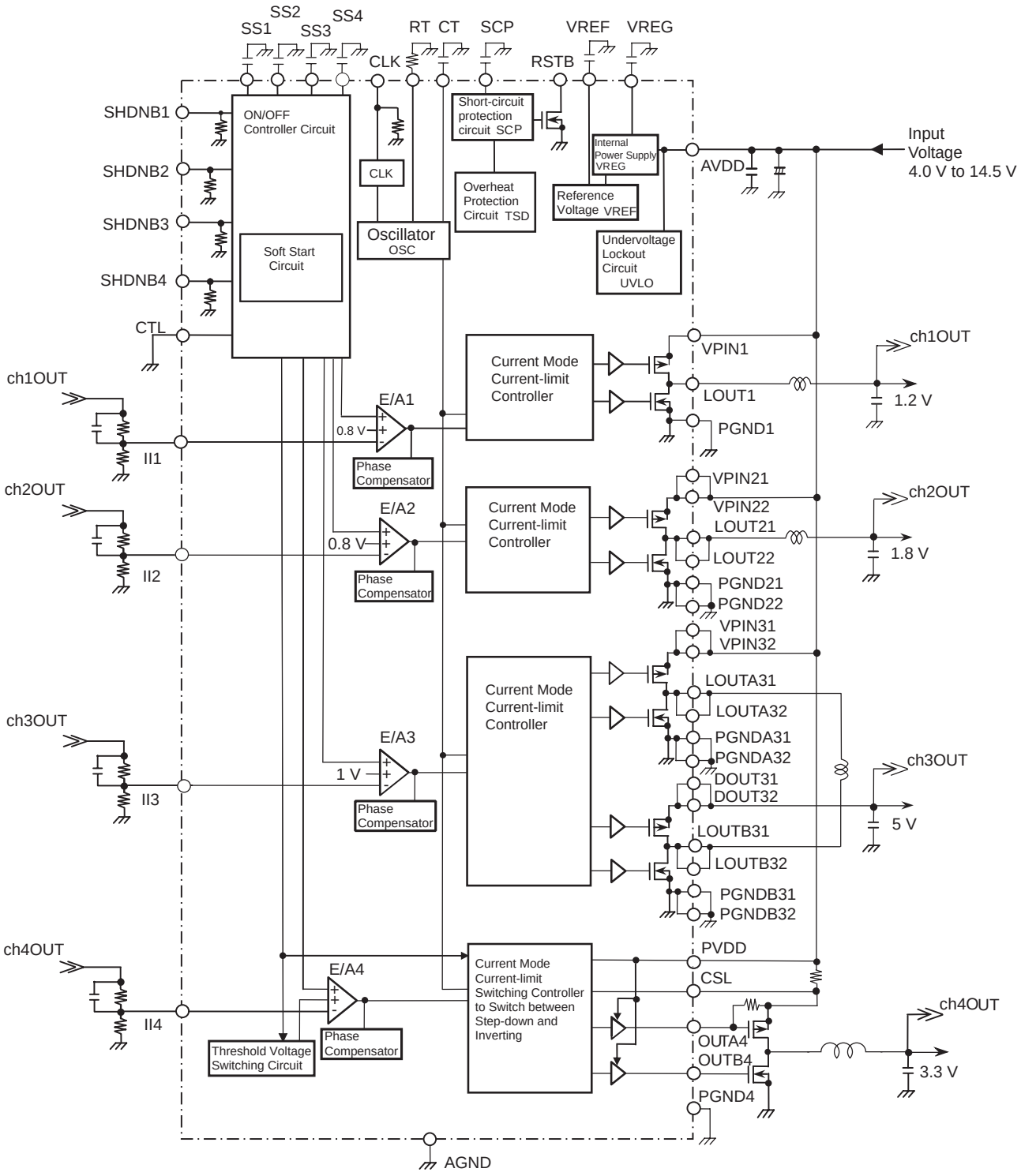
Fixed usage of control input pin

When using fixed input pins SHDNB1 to SHDNB4 and CTL input pins, connect each input to the pins listed below.

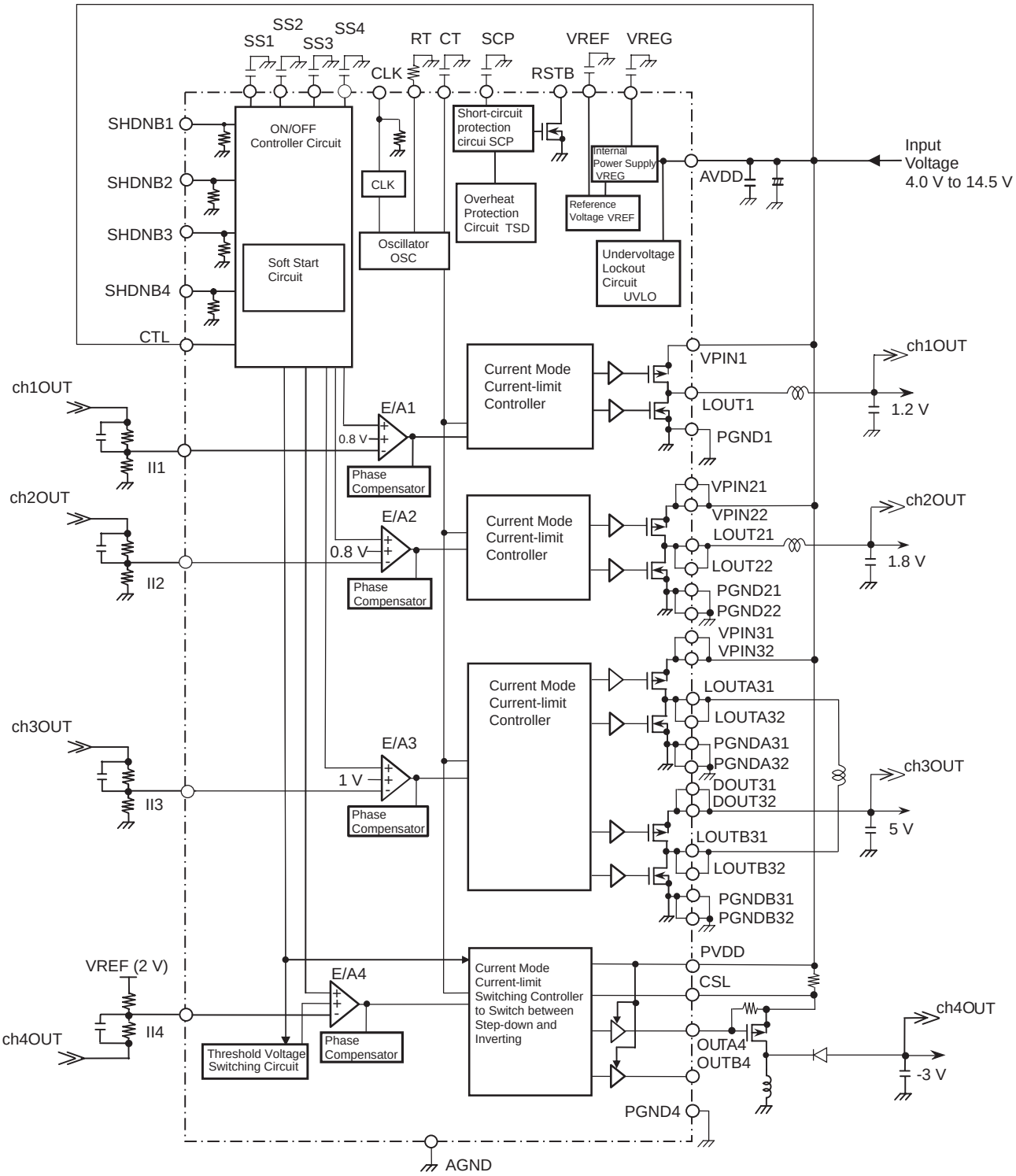
Input pin	Connect pin	
	Fixed to low level	Fixed to high level
SHDNB1	AGND	AVDD
SHDNB2	AGND	AVDD
SHDNB3	AGND	AVDD
SHDNB4	AGND	AVDD
CTL	AGND	AVDD

10. Application Circuit Example

Example 1: (ch4: Step-down operation, CTL = L)



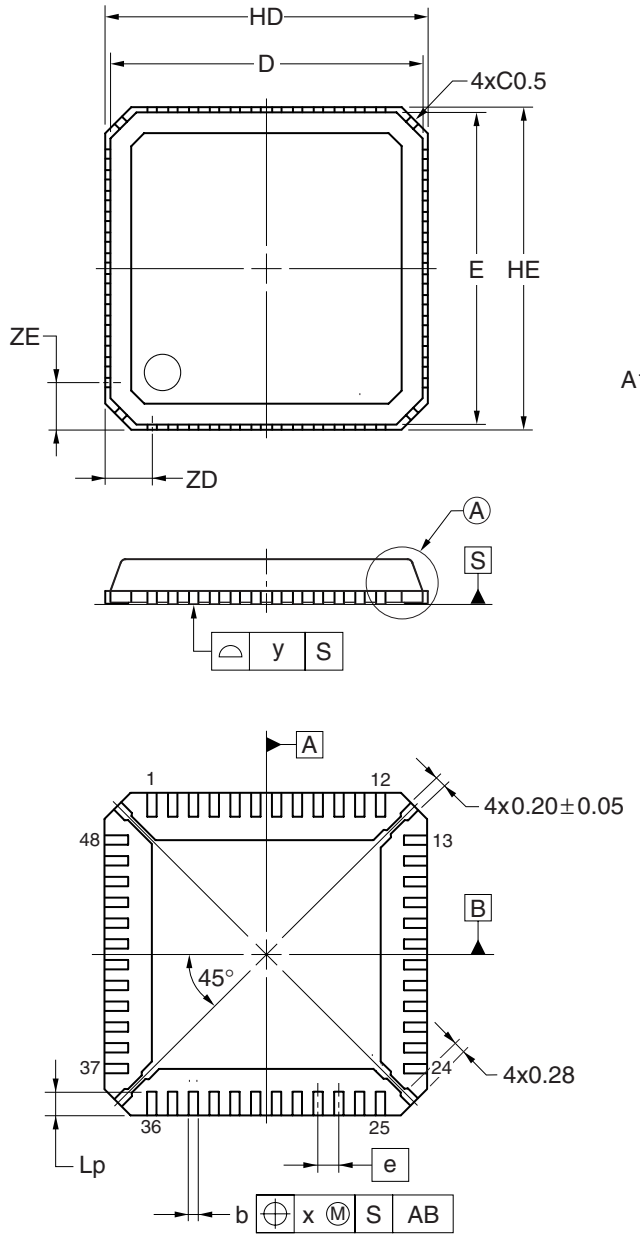
Example 2: (ch4: inverting operation, CTL = H)

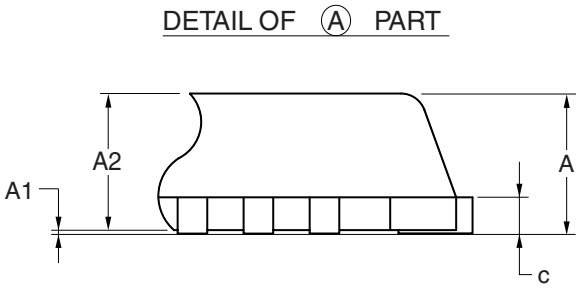


11. Package Drawing

48-PIN PLASTIC VQFN (6 mm×6 mm)
Punch Type/0.4 mm pitch/Exposed PAD

48-PIN PLASTIC VQFN (6x6)





(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.05
E	6.00±0.05
HD	6.20±0.10
HE	6.20±0.10
A	0.85±0.05
A1	$0.02^{+0.02}_{-0.015}$
A2	0.83
b	0.18±0.05
c	0.22±0.05
e	0.40
Lp	0.45±0.10
x	0.05
y	0.05
ZD	0.90
ZE	0.90

P48K9-40-4EG

12. Recommended Soldering Conditions

The μPD168807 should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact our sales representative. For technical information, see the following website.

Semiconductor Device Mount Manual (http://www2.renesas.com/pkg/en/mount/index.html)

μPD168807: 48-pin plastic VQFN

Soldering	Soldering Conditions	Recommended Method Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times. Exposure limit: 7 days *1 (after that, prebake at 125°C for 10 hours). Flux: Rosin flux with few chlorine (less than 0.2 Wt%) recommended. <Precaution> Cannot be baked in their taping package.	IR60-107-3

Note: *1. After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Revision History — μPD168807 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 31, 2010	–	First Edition Issued
2.00	Mar 18, 2011	p.22	**External clock function** Modification of Configure

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