NEC

MOS INTEGRATED CIRCUIT

μPD168802

7-CH DC-DC CONVERTER CONTROLLER IC

DESCRIPTION

The μPD168802 is a DC-DC converter controller IC that consists of an output circuit containing a 3-ch power MOSFET and an output circuit that can directly drive four channels of power MOSFETs. It is also equipped with one channel of a series regulator, so that up to eight cannels of output circuits can be configured.

In addition, by multiplexing one channel of a step-up circuit with a self-bias circuit, the minimum start voltage can be as low as 1.5 V ($AV_{DD(ST)}$), making the IC ideal with a power supply for a portable system such as a digital still camera.

FEATURES

- High-efficiency operation even with a low load thanks to employment of a PWM/PFM select circuit for ch1 (5.0 V output).
- Step-up circuit for ch2 (3.3 V output)
- Power MOSFET (ch1 to ch3)
- Phase compensator (ch1 to ch7)
- Digital soft start circuit
- High-frequency operation (300 kHz to 1000 kHz)
- Low start voltage ($AV_{DD(ST)}$ = 1.5 V min.)
- Timer latch type short-circuit protection circuit and overheat protection circuit
- Small, slim 48-pin VQFN (6 mm x 6 mm x 0.9 mm)

ORDERING INFORMATION

Part Number	Package	Packing Style
μPD168802K8-4E5-E1-AT	48-pin VQFN	Embossed taping

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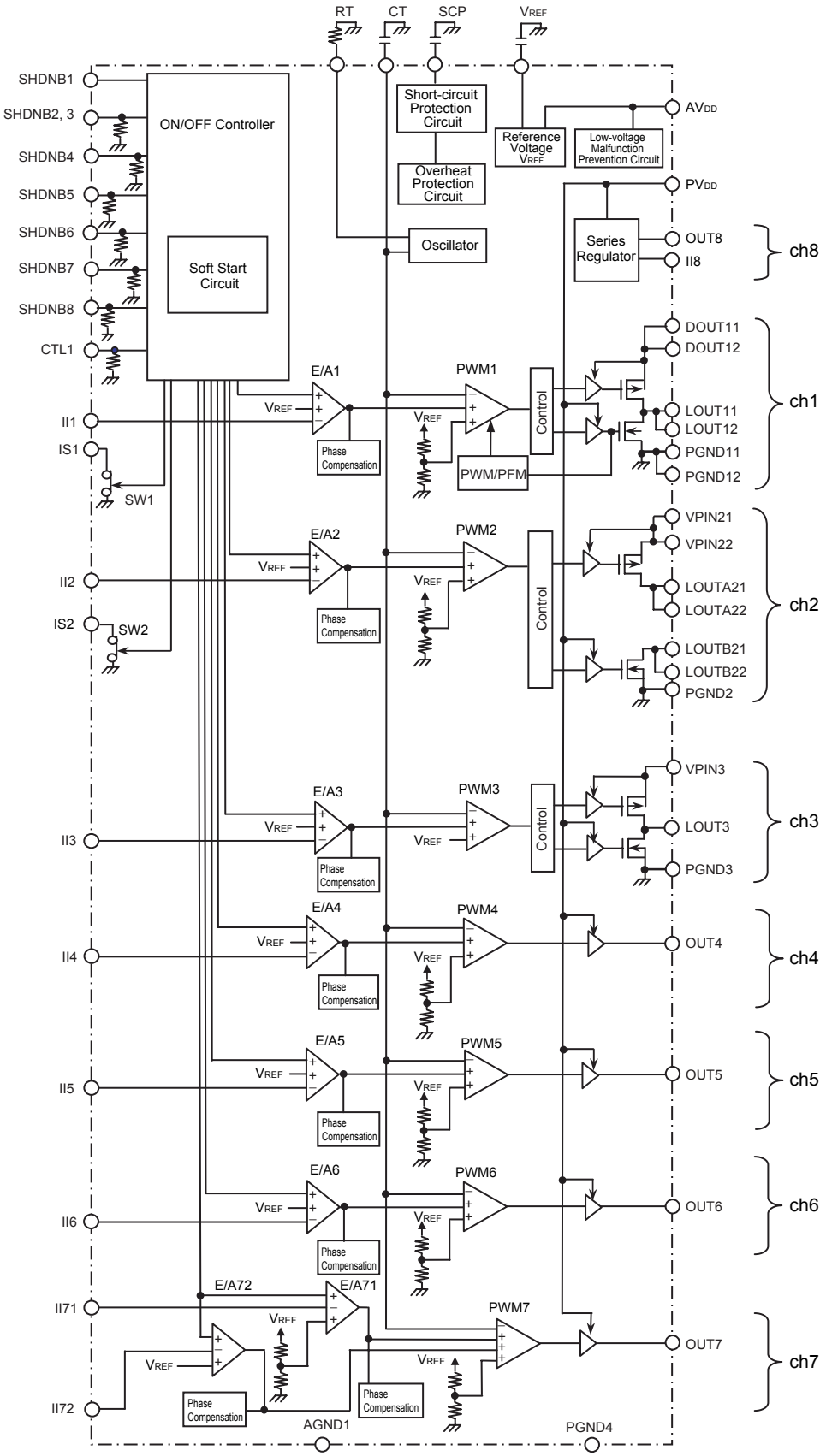
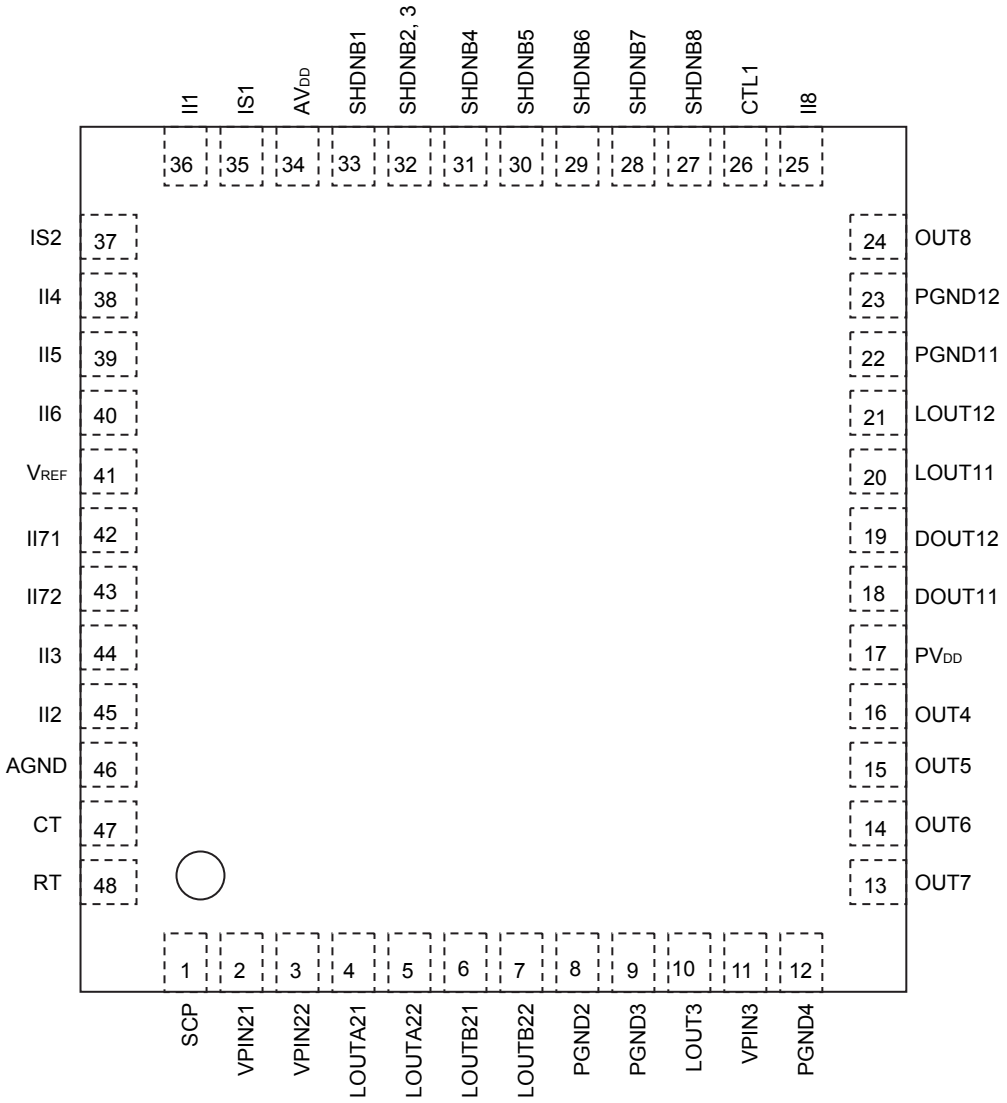
1. BLOCK DIAGRAM



2. PIN CONFIGURATION (TOP VIEW)



3. PIN FUNCTIONS

Pin No.	Symbol	Pin Name	I/O	Function
1	SCP	Short-circuit protection circuit delay capacitance	–	Capacitor connection for timer latch
2	VPIN21	Power input to output stage 21	Power supply	Output stage power input 1 to ch2
3	VPIN22	Power input to output stage 22	Power supply	Output stage power input 2 to ch2
4	LOUTA21	Output A21	Output	Inductor connection 1 for ch2A
5	LOUTA22	Output A22	Output	Inductor connection 1 for ch2A
6	LOUTB21	Output B21	Output	Inductor connection 1 for ch2B
7	LOUTB22	Output B22	Output	Inductor connection 1 for ch2B
8	PGND2	Power ground	–	Power ground
9	PGND3	Power ground	–	Power ground
10	LOUT3	Output 3	Output	Inductor connection for ch3
11	VPIN3	Power input to output stage 3	Power supply	Output stage power input 1 to ch3
12	PGND4	Power ground	–	Power ground
13	OUT7	Output 7	Output	PoMOS connection for ch7
14	OUT6	Output 6	Output	PoMOS connection for ch6
15	OUT5	Output 5	Output	PoMOS connection for ch5
16	OUT4	Output 4	Output	PoMOS connection for ch4
17	PV_{DD}	Output buffer stage power supply	Power supply	Power supply for output buffer stage
18	DOUT11	Output 11	Output	Output 1 of ch1
19	DOUT12	Output 12	Output	Output 2 of ch1
20	LOUT11	Output 11	Output	Inductor connection 1 for ch1
21	LOUT12	Output 12	Output	Inductor connection 2 for ch2
22	PGND11	Power ground	–	Power ground
23	PGND12	Power ground	–	Power ground
24	OUT8	Output 8	Output	Output 8
25	II8	Inverted input	Input	Inverted input for error amplifier of ch8
26	CTL1	Control 1	Input	PWM/PFM operation setting mode for ch1
27	SHDNB8	Shutdown 8	Input	Output ON/OFF of ch8
28	SHDNB7	Shutdown 7	Input	Output ON/OFF of ch7
29	SHDNB6	Shutdown 6	Input	Output ON/OFF of ch6
30	SHDNB5	Shutdown 5	Input	Output ON/OFF of ch5
31	SHDNB4	Shutdown 4	Input	Output ON/OFF of ch4
32	SHDNB2, 3	Shutdown 2, 3	Input	Output ON/OFF of ch2 and ch3
33	SHDNB1	Shutdown 1	Input	Output ON/OFF of ch1
34	AV_{DD}	Power supply	Power supply	Analog power supply
35	IS1	SW input	Input	Switch input of output divider resistor of ch1
36	II1	Inverted input	Input	Inverted input of error amplifier of ch1
37	IS2	SW input	Input	External Pch-MOS drive switch for ch2 (Open-drain output)
38	II4	Inverted input	Input	Inverted input of error amplifier of ch4
39	II5	Inverted input	Input	Inverted input of error amplifier of ch5
40	II6	Inverted input	Input	Inverted input of error amplifier of ch6
41	V_{REF}	Reference voltage output	Output	Reference voltage source
42	II71	Inverted input	Input	Inverted input of error amplifier of ch71
43	II72	Inverted input	Input	Inverted input of error amplifier of ch72
44	II3	Inverted input	Input	Inverted input of error amplifier of ch3
45	II2	Inverted input	Input	Inverted input of error amplifier of ch2
46	AGND	Analog ground	–	Analog ground
47	C_T	Timing capacitance	–	Capacitor connection for triangular wave generation
48	R_T	Timing resistance	–	Resistance connection for triangular wave generation

4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (Unless otherwise specified, T_A = 25°C, glass epoxy double layer substrate, 100 mm x 100 mm x 1 mm, Copper film: 50%)

Parameter	Symbol	Conditions	Rating	Unit
Analog supply voltage (AV_{DD} pin)	AV_{DD}		−0.5 to +6.5	V
Buffer stage supply voltage (PV_{DD} pin)	PV_{DD}		−0.5 to +6.5	V
VP_{IN} pin applied voltage	VP_{IN}		−0.5 to +6.5	V
LOUT11 and LOUT2 pins applied voltage	VLOUT1		−0.5 to +6.5	V
I_I pin applied voltage	V_{II}		−0.5 to AV_{DD}	V
I_S pin applied voltage	V_{IS}		−0.5 to AV_{DD}	V
SHDNB pin applied voltage	V_{SHDNB}		−0.5 to AV_{DD}	V
CTL pin applied voltage	V_{CTL}		−0.5 to AV_{DD}	V
VP_{IN2} pin sink current	IP_{IN2-}		2000	mA
VP_{IN3} pin sink current	IP_{IN3-}		1000	mA
OUT8 output source current (DC)	$I_{O8(DC)+}$		60	mA
OUT1S, OUT4, OUT5, OUT6, OUT7 output source current (DC)	$I_{O(DC)+}$		30	mA
OUT1S, OUT4, OUT5, OUT6, OUT7 output sink current (DC)	$I_{O(DC)-}$		30	mA
OUT1S, OUT4, OUT5, OUT6, OUT7 output source current (pulse)	$I_{O(pulse)+}$		200	mA
OUT1S, OUT4, OUT5, OUT6, OUT7 output sink current (pulse)	$I_{O(pulse)-}$		200	mA
DOUT11 + DOUT12 output source current (peak)	I_{DO1+}	DOUT11 + DOUT12	2500	mA
LOUT11 + LOUT12 output sink current (peak)	I_{LO1-}	LOUT11 + LOUT12	2500	mA
LOUTA21 + LOUTA22 output source current (peak)	I_{LO2+}	LOUTA21 + LOUTA22	2000	mA
LOUTB21 + LOUTB22 output sink current (peak)	I_{LO2-}	LOUTB21 + LOUTB22	2000	mA
LOUT3 output source current (peak)	I_{LO3+}		1000	mA
Total loss	P_T	$T_A \leq$ +25°C	2200[Note]	mW
Operating ambient temperature	T_A		−20 to +85	°C
Operating junction temperature	T_J		−20 to +150	°C
Storage temperature	T_{STG}		−55 to +150	°C

Note This is the value at $T_A \leq$ +25°C. Derate at −18 mW/°C at $T_A >$ +25°C.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (Unless otherwise specified, T_A = 25°C, glass epoxy double layer substrate, 100 mm x 100 mm x 1 mm, Copper film: 50%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Start voltage (AV_{DD} pin)	$AV_{DD(ST)}$		1.5			V
Analog supply voltage (AV_{DD} pin)	AV_{DD}		3.5	5.0	5.5	V
Buffer stage supply voltage (PV_{DD} pin)	PV_{DD}			AV_{DD}		V
VP_{IN2} pin applied voltage	VP_{IN2}		1.8	3.3	5.5	V
VP_{IN3} pin applied voltage	VP_{IN3}		2.5	3.3	5.5	V
LOUT11, LOUT12 pin applied voltage	VLOUT1		2.5	3.3	5.5	V
SHDNB pin applied voltage	V_{SHDNB}	SHDNB1 to SHDNB8	0		AV_{DD}	V
CTL pin applied voltage	V_{CTL}	CTL1	0		AV_{DD}	V
Oscillation frequency	f_{OSC}		300	800	1000	kHz
ch1 load current (on starting)	$I_{L(ST)}$				30	mA
ch1 load current (during PFM operation)	$I_{L(PFM)}$				5	mA
Oscillator timing resistance	R_T	R_T	0.51	1.2	5.1	kΩ
Oscillator timing capacitance	C_T	C_T	100	220	330	pF
SCP pin capacitor capacitance	C_{SCP}	SCP	0.047	0.1	0.47	μF
V_{REF} pin capacitor capacitance	C_{REF}	V_{REF}		0.1		μF

Electrical Specifications (Unless otherwise specified, T_A = 25°C, AV_{DD} = PV_{DD} = 5.0 V, VP_{IN2} = VP_{IN3} = 3.3 V, f_{OSC} = 800 kHz, PWM operation)

Total						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Standby current	$I_{BD(SHDN)}$	AI_{DD} + PI_{DD} + IP_{IN1} + IP_{IN2}, SHDNB1 to SHDNB8 = AGND		1	5	μA
Circuit operation current 1 (PWM operation)	$AI_{DD(PWM)}$	AI_{DD}, CTL1 = AV_{DD} ch1 to ch8 = "ON", II4 = 0 V II1 = II2 = II3 = II5 = II6 = II7 = II8 = AV_{DD}		3.5	5	mA
Circuit operation current 2 (PWM operation)	$PI_{DD(PWM)}$	PI_{DD}, CTL1 = AV_{DD} ch1 to ch8 = "ON", II1 = II3 = II4 = AV_{DD} II2 = II5 = II6 = II7 = II8 = 0 V, no load		3.5	5	mA
Circuit operation current 3 (PWM operation)	$AI_{DD(PFM)}$	AI_{DD}, CTL1 = AGND SHDNB2 to SHDNB8 = AGND SHDNB1 = AV_{DD}		40	80	μA
Circuit operation current 4 (PWM operation)	$PI_{DD(PFM)}$	PI_{DD}, CTL1 = AGND SHDNB2 to SHDNB8 = AGND SHDNB1 = AV_{DD}, no load		2	5	μA
On starting						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference voltage	$V_{REF(ST)}$	AV_{DD} = PV_{DD} = 1.8 V, I_{REF} = 0 mA	0.9	1.0	1.01	V
Oscillation frequency	$f_{OSC(ST)}$	AV_{DD} = PV_{DD} = 1.8 V, C_T = 220 pF, R_T = 1.2 kΩ	50	800	880	kHz
Short-circuit protection circuit, input detection voltage	$V_{THSCP(ST)}$	AV_{DD} = PV_{DD} = 1.8 V, ch1 load short-circuited, II1 pin	0.4	0.5	0.6	V
Short-circuit protection circuit, DLY detection voltage	$V_{THDLY(ST)}$	AV_{DD} = PV_{DD} = 1.8 V, ch1 load short-circuited, LY pin	0.6	0.9	1.2	V
Short-circuit protection circuit, short circuit source current	$I_{OUT(ST)}$	AV_{DD} = PV_{DD} = 1.8 V, ch1 load short-circuited	0.45	0.80	1.15	μA
Soft start time	$t_{SS(ST)}$	AV_{DD} = PV_{DD} = 1.8 V, ch1		15		ms
During PFM operation						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum duty	$D_{MAX.(PFM)}$	No load, PFM operation		35		%

Electrical Specifications (Unless otherwise specified, T_A = 25°C, AV_{DD} = PV_{DD} = 5.0 V, VP_{IN2} = VP_{IN3} = 3.3 V, f_{OSC} = 800 kHz, PWM operation)

Reference voltage block						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference voltage	V_{REF}	I_{REF} = 0 mA	0.99	1.0	1.01	V
Input stability	$V_{REF(REGIN)}$	AV_{DD} = PV_{DD} = 3.5 to 5.2 V		5	10	mV
Load stability	$V_{REF(REGL)}$	I_{REF} = 0 to 1.0 mA		10	20	mV
Low-voltage malfunctioning prevention circuit						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation start voltage during rise time (ch2 to ch7)	$AV_{DD(L-H)2-7}$	AV_{DD} pin voltage detected	2.1	2.5	2.9	V
Operation stop voltage (ch2 to ch7)	$AV_{DD(H-L)2-7}$	AV_{DD} pin voltage detected	1.8	2.2	2.6	V
Short-circuit protection circuit						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I_{I1} input detection voltage (ch1)	$V_{TH(II)1}$	I_{I1} pin	0.4	0.5	0.6	V
I_{I2} input detection voltage (ch2)	$V_{TH(II)2}$	I_{I2} pin	0.7	0.8	0.9	V
I_{I3} input detection voltage (ch3)	$V_{TH(II)3}$	I_{I3} pin	0.7	0.8	0.9	V
I_{I4} input detection voltage (ch4)	$V_{TH(II)4}$	I_{I4} pin	0.7	0.8	0.9	V
I_{I5} input detection voltage (ch5)	$V_{TH(II)5}$	I_{I5} pin	0.7	0.8	0.9	V
I_{I6} input detection voltage (ch6)	$V_{TH(II)6}$	I_{I6} pin	0.7	0.8	0.9	V
I_{I7-2} input detection voltage (ch7)	$V_{TH(FB)7-2}$	I_{I7-2} pin	0.1	0.2	0.3	V
DLY detection voltage	$V_{TH(DLY)}$	C_{DLY} pin	0.6	0.9	1.2	V
Short circuit source current	I_{OUT}		0.6	0.85	1.2	μA
Oscillation block						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level threshold voltage	$V_{TH(L)}$		0.1	0.2	0.3	V
High-level threshold voltage	$V_{TH(H)}$		0.5	0.6	0.7	V
Frequency setting accuracy	f_{OSC}	C_T = 220 pF, R_T = 1.2 kΩ		±10		%
Input stability	Δf_{OSC}	C_T = 220 pF, R_T = 1.2 kΩ, AV_{DD} = 3.5 to 5.2 V		±3		%
Soft start block						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Soft start time	t_{SS}	ch2 to ch7		4		ms
PWM block						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum duty 1	$D_{MAX.1}$	ch1, ch2 stepped up, ch4, ch5, ch6, ch7		85		%
Maximum duty 2	$D_{MAX.2}$	ch2 stepped down, ch3		100		%

Electrical Specifications (Unless otherwise specified, T_A = 25°C, AV_{DD} = PV_{DD} = 5.0 V, VP_{IN2} = VP_{IN3} = 3.3 V, f_{OSC} = 800 kHz, PWM operation)

E/A block (ch1 to ch2)						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
E/A 1 input threshold voltage	V_{ITH1}	Including input offset	0.988	1.008	1.028	V
E/A 2 input threshold voltage	V_{ITH2}	Including input offset	0.98	1	1.02	V
E/A 3 input threshold voltage	V_{ITH3}	Including input offset	0.988	1.008	1.028	V
E/A 4 input threshold voltage	V_{ITH4}	Including input offset	0.579	0.604	0.629	V
E/A 5 input threshold voltage	V_{ITH5}	Including input offset	0.991	1.002	1.013	V
E/A 6 input threshold voltage	V_{ITH6}	Including input offset	0.98	1	1.02	V
E/A 7-1 input threshold voltage	V_{ITH7-1}	Including input offset	0.381	0.406	0.431	V
E/A 7-2 input threshold voltage	V_{ITH7-2}	Including input offset	0.988	1.008	1.028	V
Input block (ch1, ch4)						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IS1 input ON resistance	R_{ONIS1}	IS1 pin, IS1 = 100 μA		100	200	Ω
IS2 input ON resistance	R_{ONIS2}	IS2 pin, IS2 = 100 μA		150	300	Ω
IS2 ON operation start voltage	$V_{PIN2(H-L)}$	Low-level threshold (falling) voltage of VPIN21 and VPIN22 pins	2.5	2.72	2.94	V
IS2 OFF operation voltage	$V_{PIN2(L-H)}$	High-level threshold (rising) voltage of VPIN21 and VPIN22 pins	2.98	3.2	3.41	V
Output block (ch1)						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
P-ch output ON resistance	R_{on-p1}	I_O = 100 mA		0.2	0.4	Ω
N-ch output ON resistance	R_{on-n1}	I_O = −100 mA		0.2	0.4	Ω
Output block (ch2)						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
P-ch output ON resistance	R_{on-p2}	I_O = 100 mA		0.2	0.4	Ω
N-ch output ON resistance	R_{on-n2}	I_O = −100 mA		0.2	0.4	Ω
Output block (ch3)						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
P-ch output ON resistance	R_{on-p3}	I_O = 100 mA		0.4	0.5	Ω
N-ch output ON resistance	R_{on-n3}	I_O = −100 mA		0.4	0.5	Ω
Output block (ch4 to ch7)						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output ON resistance	R_{on4-7}	I_O = 20 mA		10	20	Ω
Series regulator block (ch8)						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OUT8 output ON resistance	R_{on8}	I_O = 50 mA		10	20	Ω
Input threshold voltage	V_{ITH8}	I_O = 0 mA, including offset	0.97	1.0	1.03	V
ON/OFF controller block						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Threshold voltage	$V_{TH(SHDNB)}$	SHDNB1 to SHDNB7, CTL1	0.6		1.4	V
Input pull-down resistance	R_{IND}	SHDNB2 to SHDNB7, CTL1	200	400	700	kΩ

5. OUTPUT CONTROL BLOCK

(1) CTL1: PWM/PFM operation setting mode of ch1

Signal	PWM/PFM operation setting of ch1
L	PFM operation, SW1 = ON (**Caution The μPD168802 performs a PWM operation on starting. ch2 to ch8, other than ch1, do not operate.**)
H	PWM operation, SW1 = OFF

Remark L: Low level, H: High level

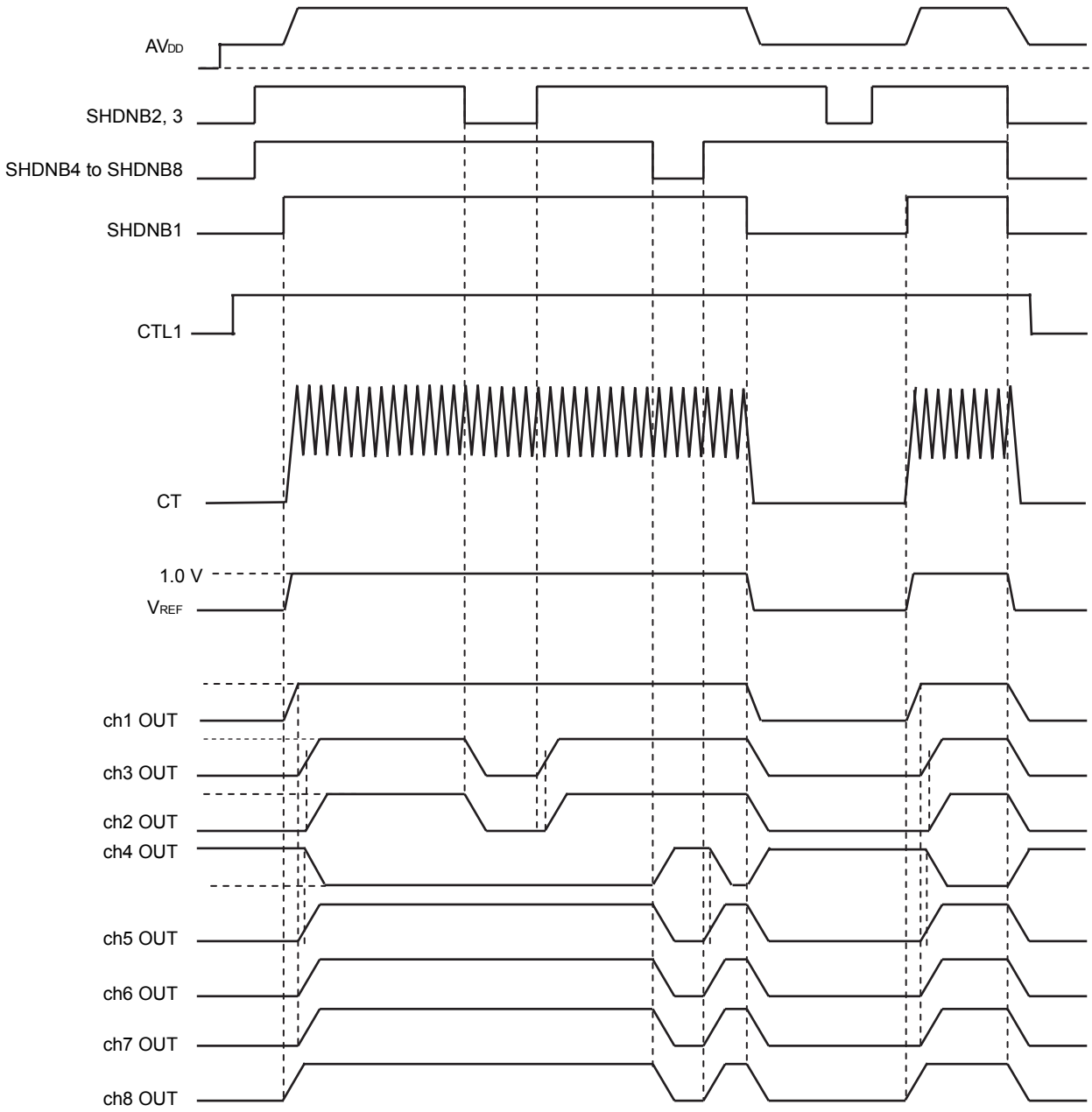
(2) SHDNB: ON/OFF setting mode (when CTL1 = H)

SHDNB1	SHDNB2, SHDNB3	SHDNB4	SHDNB5	SHDNB6	SHDNB7	SHDNB8	ch1	ch2, ch3	ch4	ch5	ch6	ch7	ch8
L	L	L	L	L	L	L	OFF						
H	L	L	L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF
	H	H	H	H	H	H		ON	ON	ON	ON	ON	ON

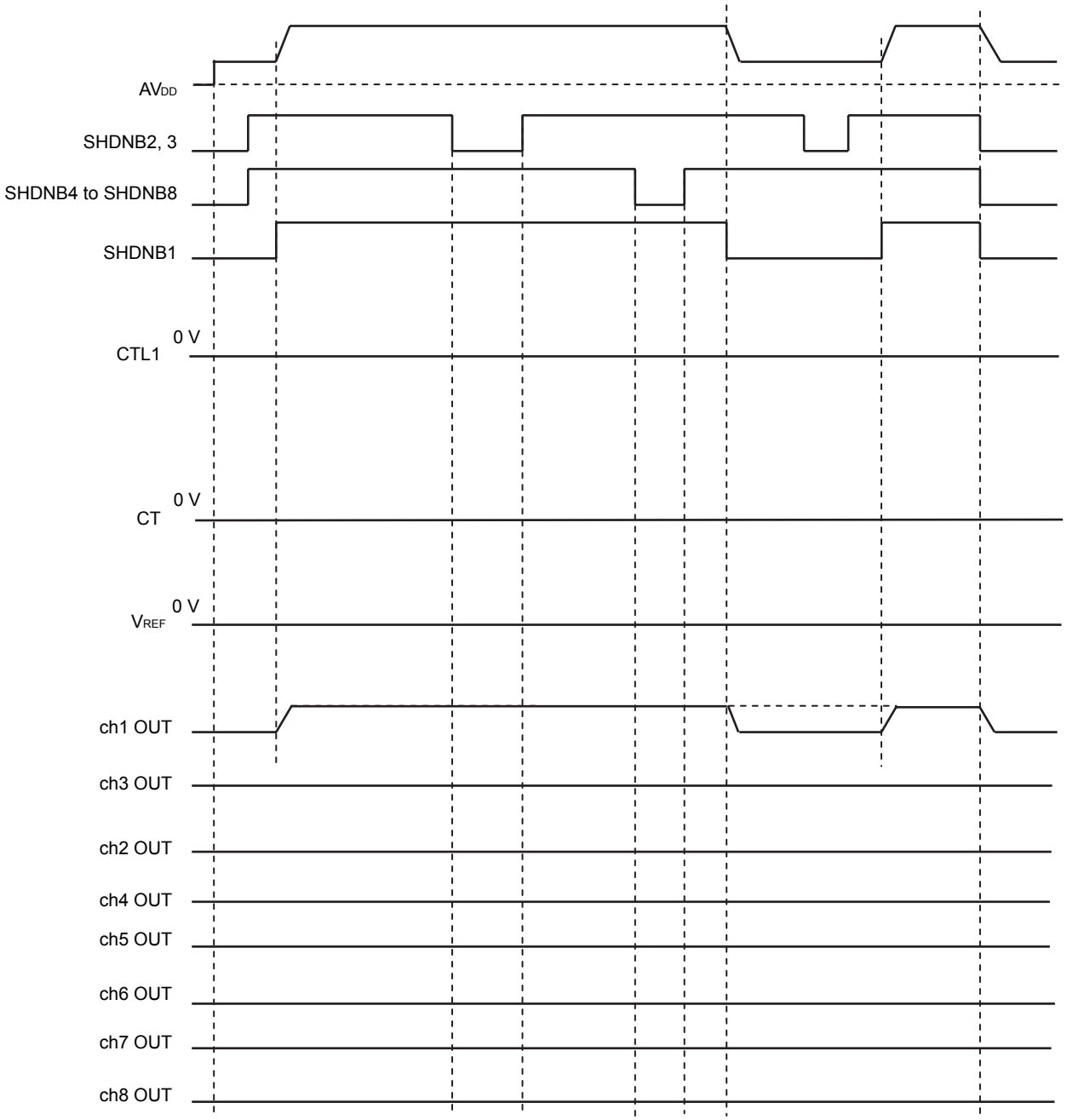
Remark L: Low level, H: High level

6. TIMING CHART

(1) PWM mode



(2) PFM mode


AVDD
SHDNB2, 3
SHDNB4 to SHDNB8
SHDNB1
0 V
CTL1
0 V
CT
0 V
VREF
ch1 OUT
ch3 OUT
ch2 OUT
ch4 OUT
ch5 OUT
ch6 OUT
ch7 OUT
ch8 OUT

7. OPERATION OF EACH BLOCK

7.1 Reference Voltage Block

This block outputs a reference voltage (1.0 V (TYP.)) that is a voltage supplied from the AV_{DD} pin (pin 34) and is temperature-compensated. The reference voltage is used for each internal circuit and a current of up to 1 mA can be output to an external circuit from the V_{REF} pin (pin 41).

The reference voltage block stops when ch1 performs a PFM operation.

7.2 Oscillator Block

The oscillator block spontaneously oscillates when a timing capacitance and a timing resistance are respectively connected to the CT pin (pin 47) and RT pin (pin 48), and outputs a symmetrical triangular wave with an amplitude of 0.2 to 0.6 V (TYP.) to the CT pin (pin 47). This triangular wave is supplied to the inverted input pin of the PWM comparator.

The oscillator block stops when ch1 performs a PFM operation.

7.3 E/A Block (Error amplifier)

The circuit configuration of all error amplifiers E/A1, E/A2, E/A3, E/A4, E/A5, E/A6, E/A7-1, and E/A7-2 is identical. All E/As have an internal phase compensator.

Caution The phase may be compensated by using an external component. For details, refer to 8 ADVICE ON DESIGNING.

Pin II inputs an inverted signal to the E/A block. The input threshold voltages of the E/A block are about 1.0 V for E/A1, E/A2, E/A3, E/A5, E/A6, and E/A7-2; 0.604 V (TYP.) for E/A2; and 0.406 V (TYP.) for E/A7-1.

7.4 PWM Block (PWM comparator)

The PWM comparator compares a triangular wave signal and an E/A output signal (or maximum duty) and controls output ON duty. The maximum duty is 85% (TYP.) at ch4, ch5, ch6, and ch7 when ch1 and ch2 are stepped up, and 100% at ch3 when ch2 is stepped down.

7.5 Output Circuit Block

The output circuit block of ch1 to ch3 has an internal power MOSFET. The output current capacity of ch1 is 2.5 A (MAX.) at the peak of switching, that of ch2 is 2.0 A (MAX.), and that of ch3 is 1.0 A (MAX.).

The output circuit block of ch4 to ch7 is of push-pull configuration and can directly drive a power MOSFET. The output current capacity is 200 mA (MAX.) in pulse and 30 mA (MAX.) in DC.

7.6 Low-Voltage Malfunctioning Prevention Circuit Block

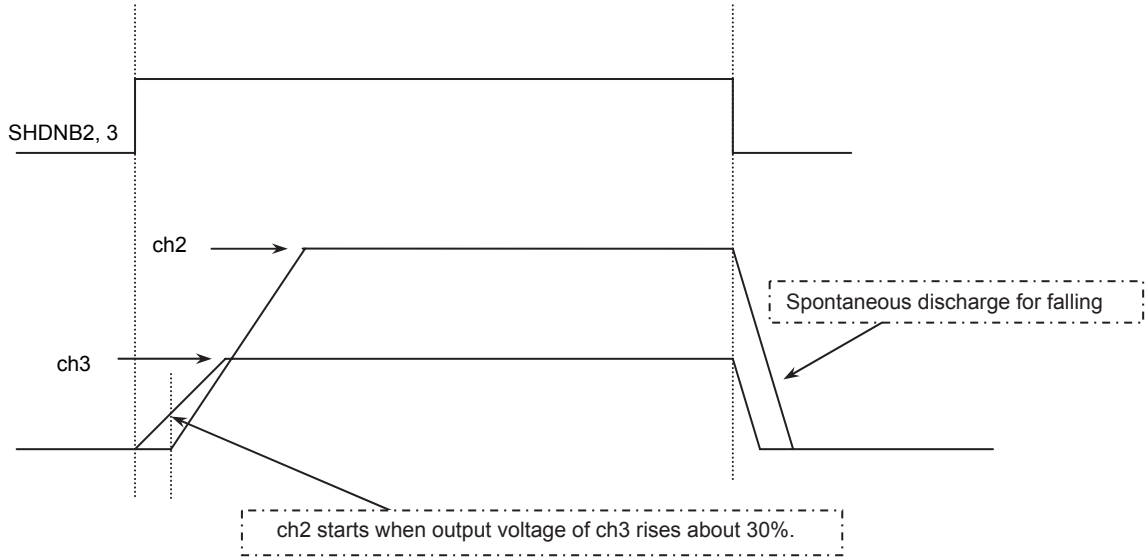
The low-voltage malfunctioning prevention circuit shuts down the IC to prevent it from malfunctioning when the supply voltage of the AV_{DD} pin (pin 34) drops. Because the voltage from the AV_{DD} pin (pin 34) is detected, ch1 which is multiplexed with self bias, and series regulator ch8 are not connected to the low-voltage malfunctioning prevention circuit.

7.7 ON/OFF Control Block

This circuit can turn on/off the output voltage of each channel by using the SHDNB1 to SHDNB8 pins and an external signal. When the SHDNB1 to SHDNB8 pins are made low, a shut-down circuit operates, shutting down the output of each channel. When the SHDNB1 to SHDNB8 pins are made high, the shut-down circuit stops, ch1 to ch7 are soft-started and their output voltage rises, and the output voltage of ch8 instantaneously rises.

ch2 and ch3 have an internal start sequence circuit. When SHDNB2, 3 pin (pin 32) is made high, the output voltage of ch3 starts rising. When the output voltage of ch3 rises about 30%, ch2 starts rising. At this time, the output voltage of ch2 does not exceed the output voltage of ch3 since ch2 has started and until soft start is completed (Figure 7-1).

Figure 7-1.



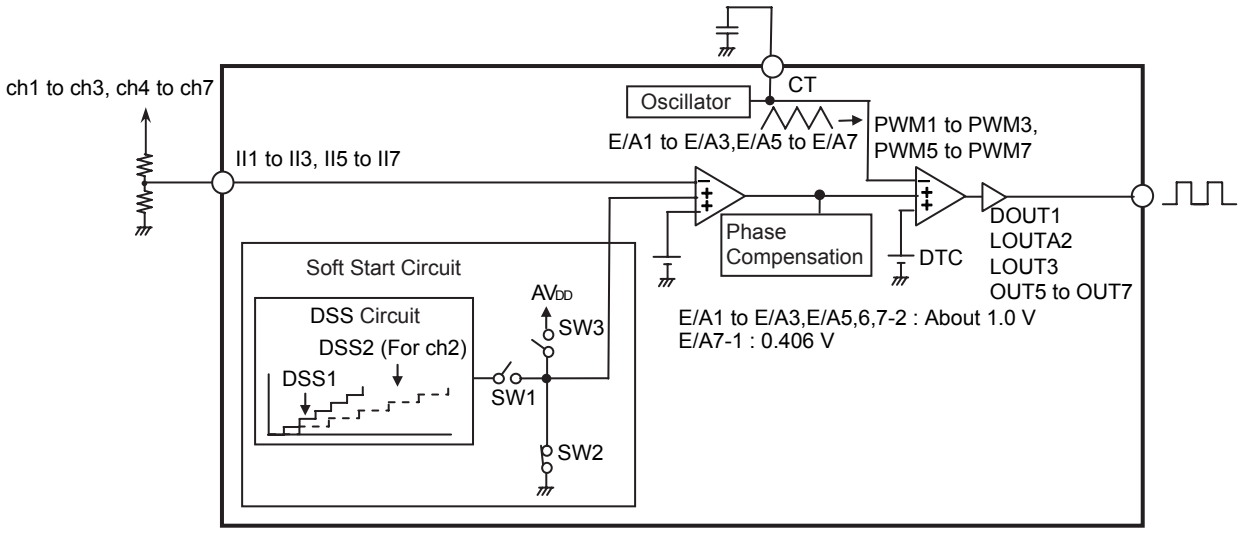
In addition, how to control the DC-DC converter of ch1 can be selected by using the CTL1 pin (pin 26). When the CTL1 pin is made low, ch1 operates in the PFM mode; when the CTL1 pin is made high, ch1 operates in the PWM mode. In the PFM mode (CTL1 pin = low), the reference voltage and oscillator stop. Therefore, ch2 to ch8 do not turn ON even if SHDNB2 to SHDNB8 are made high.

7.8 Soft Start Circuit Block (Soft start circuit for step-up or step-down DC-DC converter output)

Soft start is realized by gradually increasing the E/A threshold voltage, using the voltage that is generated by the DSS circuit and increases in 64 steps. Two DSS circuits are provided: DSS1 determines the soft start time of ch1 and ch3 to ch7, and DSS2 determines the soft start time of ch2. The time determined by DSS2 is about twice the time determined by DSS1 (Figure 7-2).

On starting, the DSS voltage is connected to a non-inverted input of an E/A. By increasing the non-inverted input voltage of the E/A from 0 V, the output ON duty is gradually widened and soft start is executed (Figure 7-3).

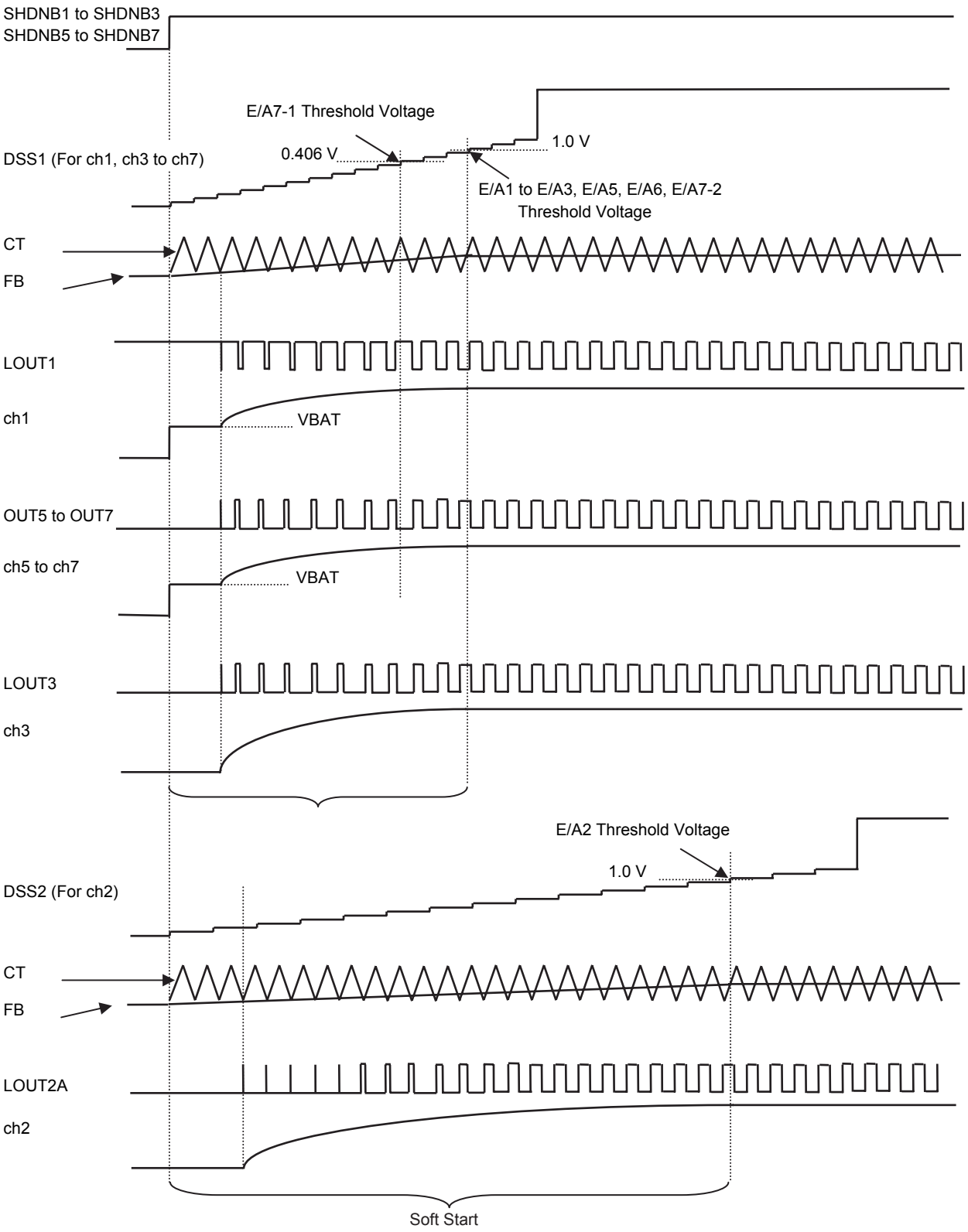
Figure 7-2



	DSS Circuit	SW1	SW2	SW3
Before starting	OFF	OFF	ON	OFF
During starting	ON	ON	OFF	OFF
After starting	OFF	OFF	OFF	ON

Caution This figure does not indicate the start timing of each ch.

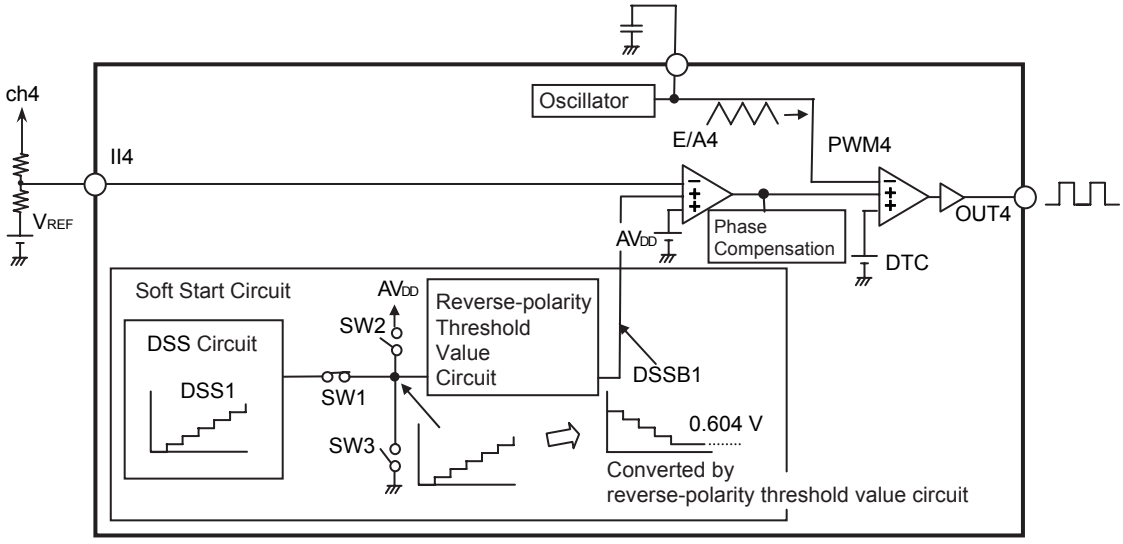
Figure 7-3



7.9 Soft Start Circuit Block (Soft start circuit of reverse-polarity DC-DC converter output)

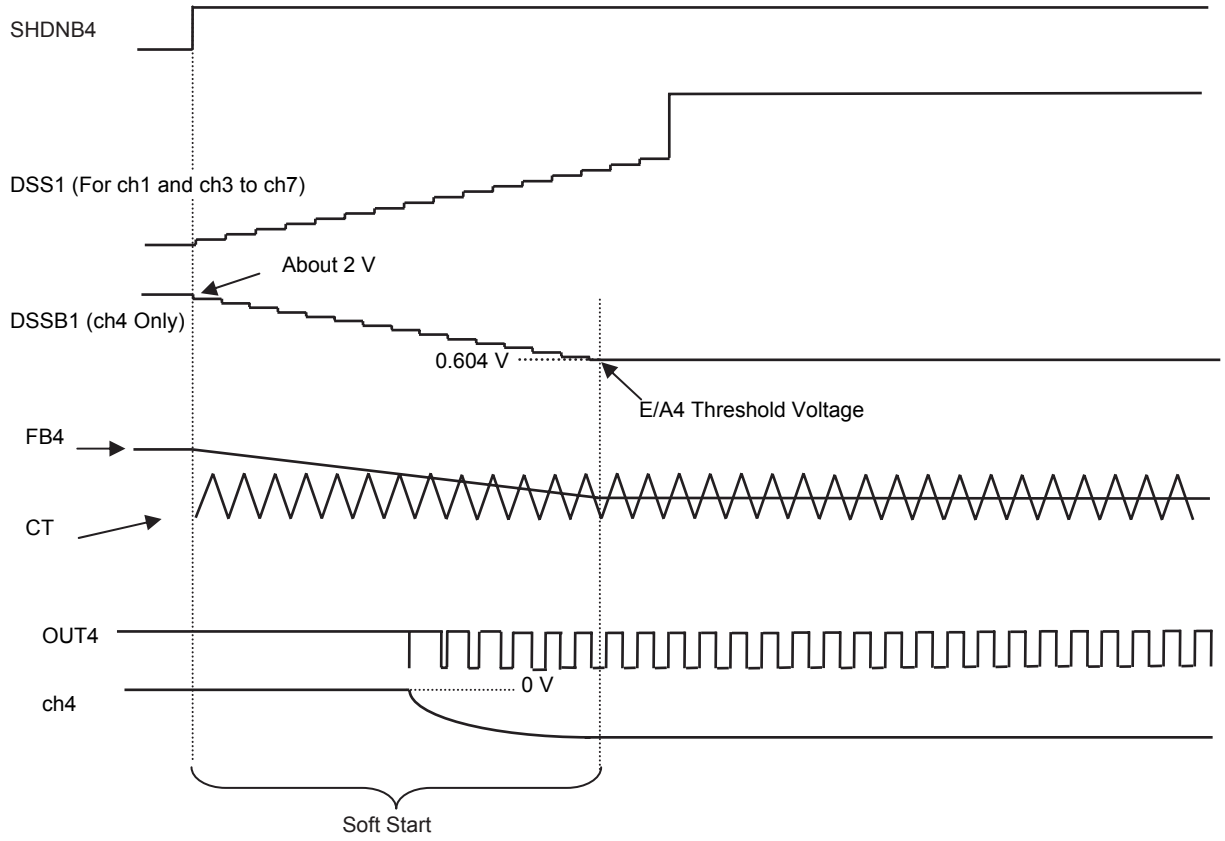
Soft start of reverse polarity (ch4) is realized by gradually decreasing the E/A threshold voltage. The DSS1 voltage is converted into a low voltage by a reverse-polarity threshold circuit. This converted voltage is connected to a non-inverted input of an E/A, and soft start is executed by gradually decreasing the non-inverted input voltage of the E/A from about 2 V and thus gradually widening the output ON duty (Figure 7-4, Figure 7-5).

Figure 7-4



	DSS Circuit	SW1	SW2	SW3
Before starting	OFF	OFF	ON	OFF
During starting	ON	ON	OFF	OFF
After starting	OFF	OFF	OFF	ON

Figure 7-5


SHDNB4
DSS1 (For ch1 and ch3 to ch7)
About 2 V
DSSB1 (ch4 Only)
0.604 V
E/A4 Threshold Voltage
FB4
CT
OUT4
0 V
ch4
Soft Start

7.10 Short-circuit Protection Circuit (Timer latch type)

When ch1 to ch7, which are output voltages of a DC-DC converter, drop (when the voltage of ch4 rises), the inverted input pin voltage of an E/A that feeds back the output also drops (the voltage of ch4 rises). If this inverted input pin voltage falls below the input detection voltage (E/A1 = VTH1 = 0.5 V, E/A2 = VTH2 = 0.8 V, E/A3 = VATH3 = 0.8 V, E/A4 = VTH4 = 0.8 V, E/A5 = VTH5 to 0.8 V, E/A6 = VTH6 = 0.8 V, E/A7-2 = VTH7-2 = 0.2 V. E/A7-1 does not have a detection circuit of the short-circuit protection circuit.) of the short-circuit protection circuit, a timer circuit operates, starting charging of the capacitor (C_{SCP}) connected to the SCP pin (pin 31). When the voltage of the capacitor connected to the SCP pin (pin 1) reaches 0.9 V (TYP.), all the output signals of the IC are latched to off. During the PFM operation (CTL1 = low), the short-circuit protection circuit does not operate (Figure 7-6 to Figure 7-9).

If the inverted input pin voltage of one of the E/As of ch1 to ch7-2 is lower than the input detection voltage of the short-circuit protection circuit, charging the capacitor connected to the SCP pin (pin 1) goes on (Figure 7-10).

When the short-circuit protection circuit operates, the latch circuit is reset if the supply voltage (AV_{DD}) is once lowered to the GND level, if the SHDNB1 pin (pin 33) goes low, or if the CTL1 pin (pin 26) goes low.

Figure 7-6

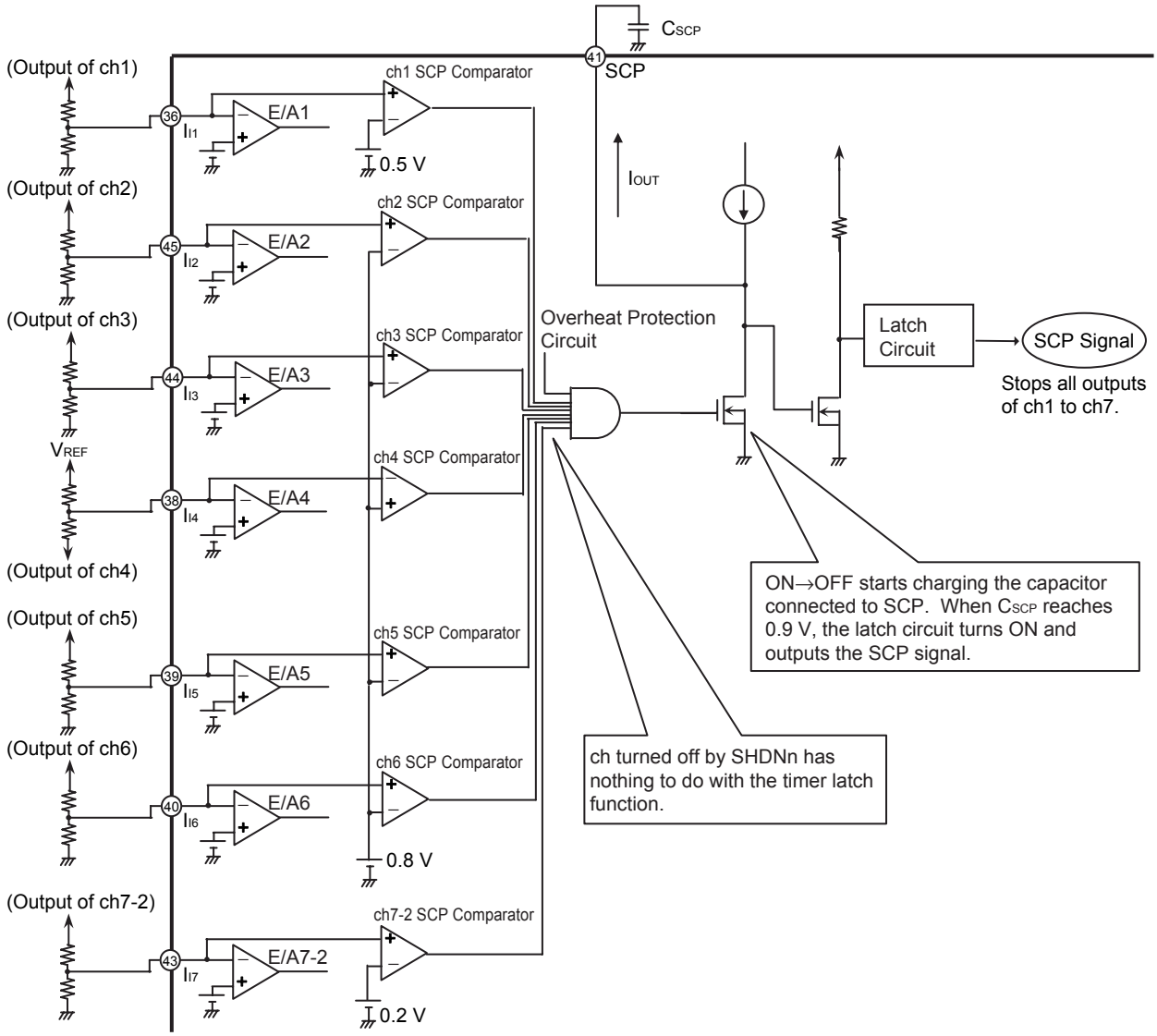


Figure 7-7

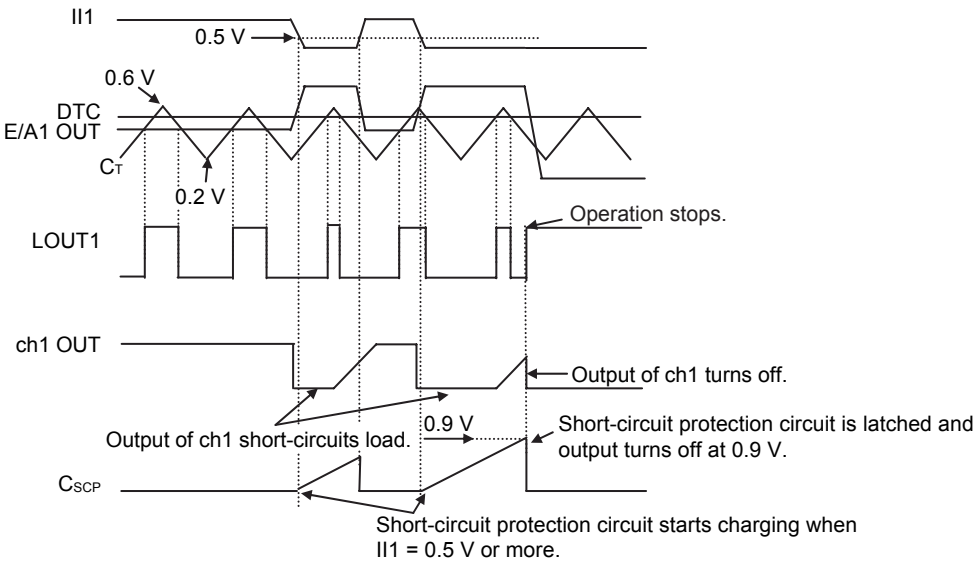


Figure 7-8

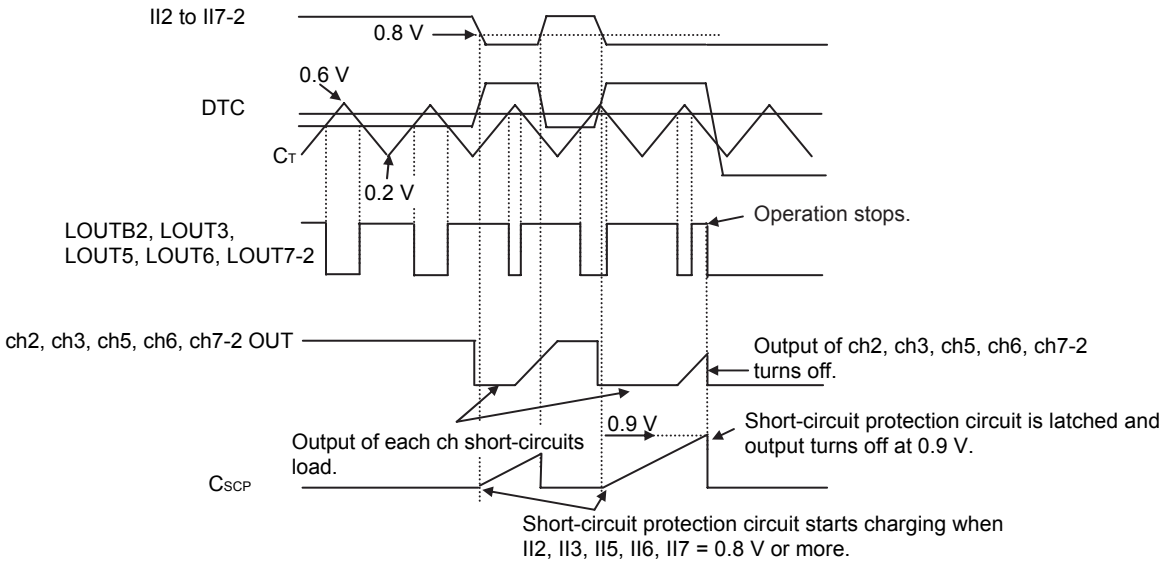


Figure 7-9

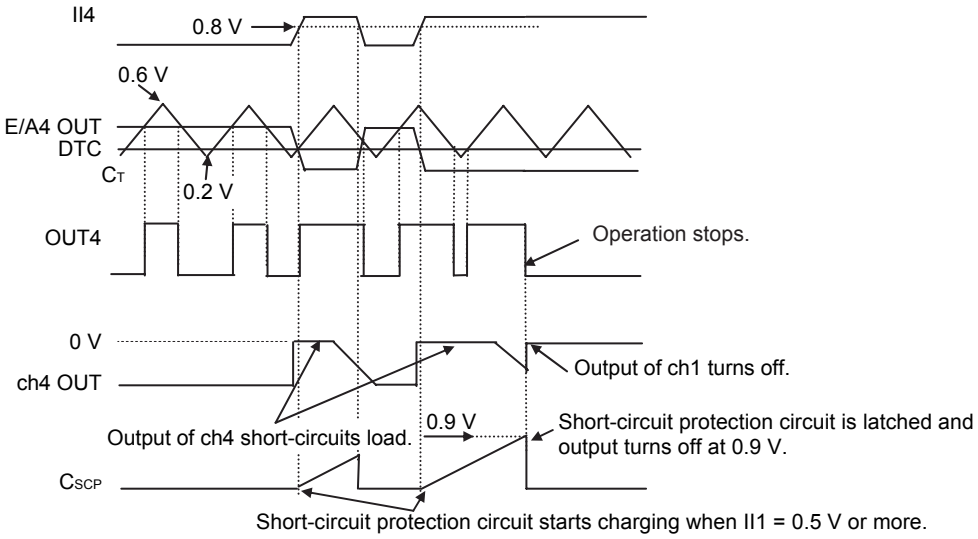
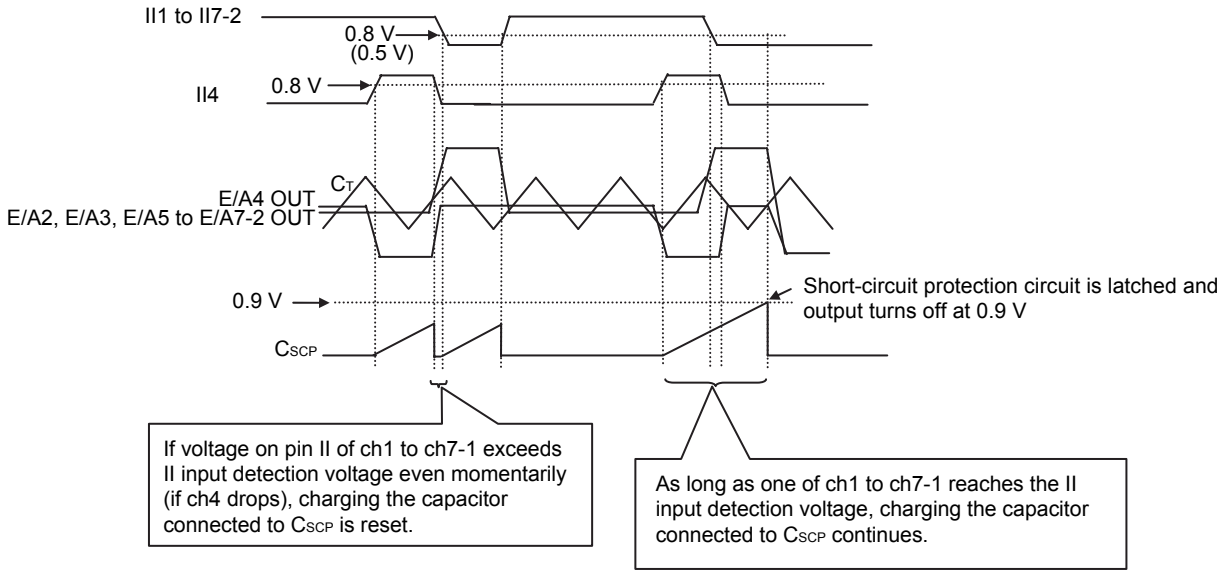


Figure 7-10



7.11 Overheat Protection Circuit

This IC has an internal temperature detector that activates the short-circuit protection circuit when the internal temperature of the IC exceeds 150°C, and latches ch2 to ch7 outputs other than ch1 and ch8 to off. During PFM operation (CTL1 = high), the overheat protection circuit does not operate.

When the overheat protection circuit operates, the latch circuit is reset if the supply voltage (AV_{DD}) is once lowered to the GND level, if the SHDNB1 pin (pin 33) goes low, or if the CTL1 pin (pin 26) goes low.

7.12 Series Regulator Block (ch8)

The series regulator can output the voltage set by the II8 pin (pin 25) (for how to set this voltage, refer to **8 ADVICE ON DESIGNING**), inputting a power from the PV_{DD} pin (pin 17). The ON resistance between input and output is 10 Ω (typ.), and the load current is 60 mA.

7.13 SW1 and SW2 Blocks

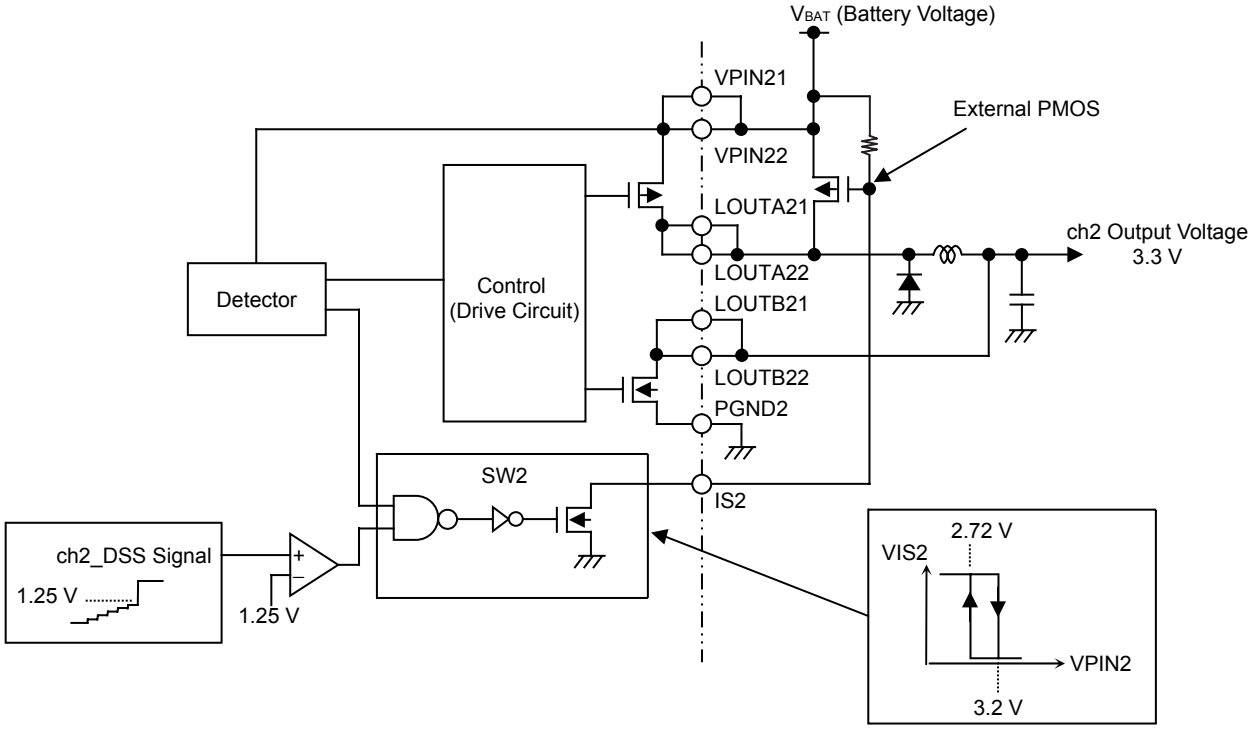
SW1 operates in association with CTL1. It turns on when CTL1 is low, and off when CTL1 is high. Because SW1 can connect the IS1 pin (pin 35) to AGND, it is used to change the output voltage of ch1 between the PFM and PWM operations.

SW2 operates in association with SHDNB23 and the input voltage of VPIN21 and VPIN22. It turns off when SHDNB23 is low, or when SHDNB23 is high and the input voltage of VPIN21 and VPIN22 is 3.2 V (TYP.) or higher. It turns on when SHDNB23 is high and when the input voltage of VPIN21 and VPIN22 is 2.72 V (TYP.) or lower.

SW2 is a set that requires low-voltage operation such as driven by battery power. It is used for increasing the load current capability of ch2. The load current capability when inputting the low-voltage can be increased by connecting external power MOSFETs between VPIN21 and VPIN22, and LOUT21 and LOUT22 as shown below. The IS2 pin (pin 37) is an open-drain output. SW2 does not operate during the software startup.

- ch2 Circuit

Figure 7-11



7.14 PWM/PFM Block

The switching operation of PWM and PFM is shown in Figure 7-12, and the block diagram of this block is shown in Figure 7-13.

Figure 7-12

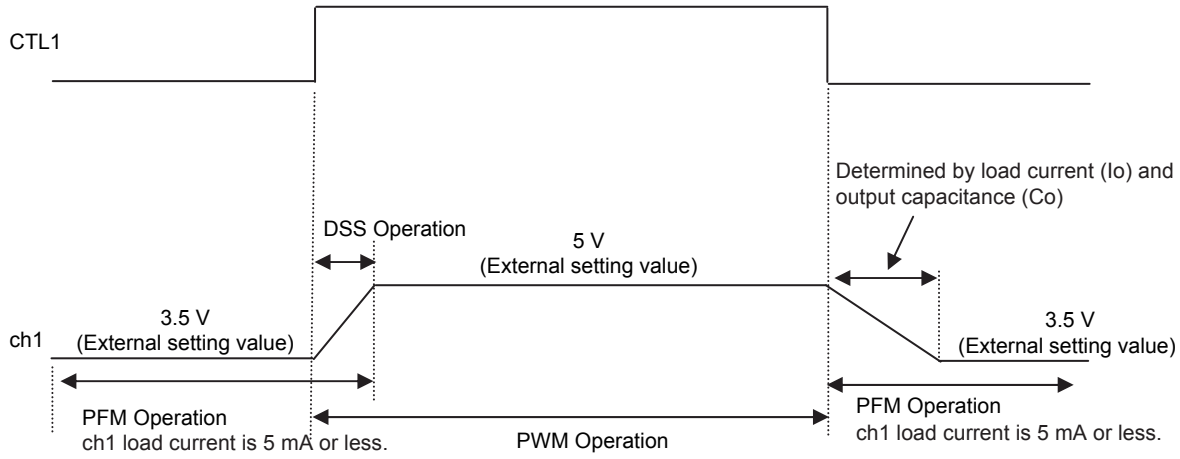
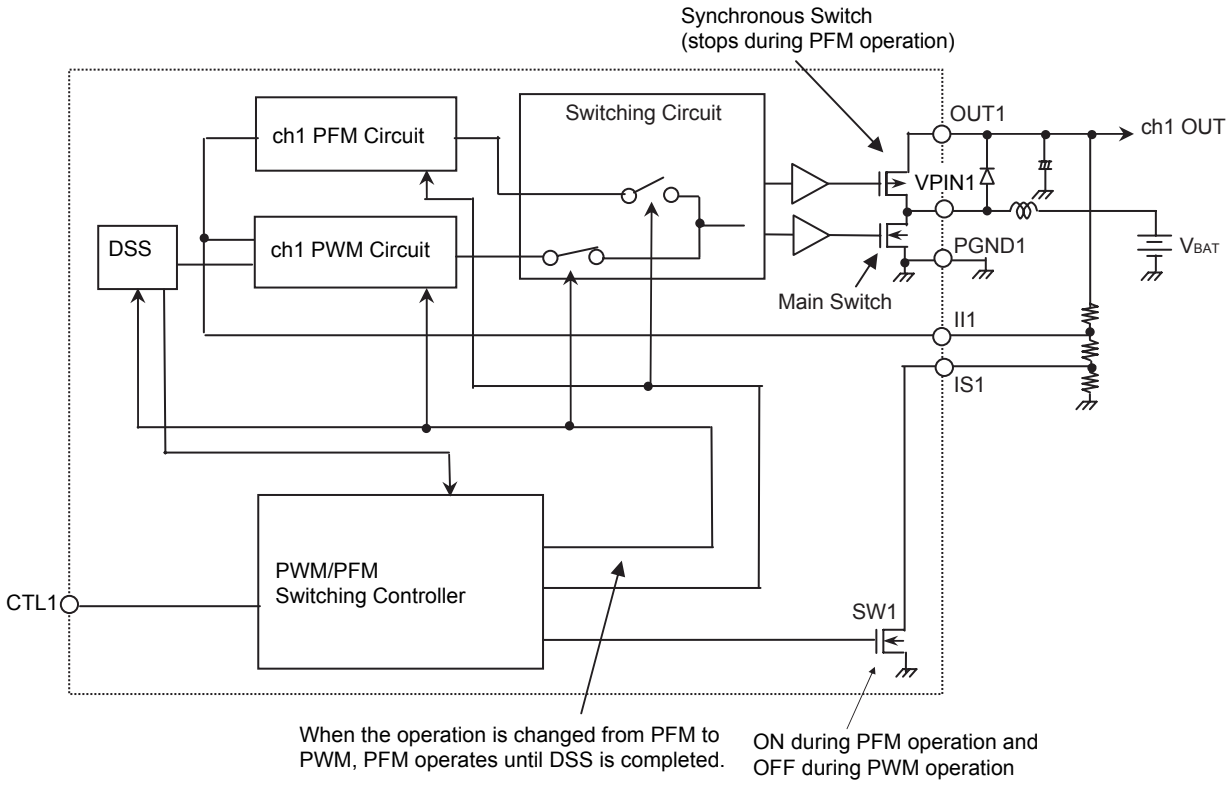


Figure 7-13



7.15 ch7 Block

The block diagram of ch7 is shown in Figure 7-14, and timing chart of this block is shown in Figure 7-15.

Figure 7-14

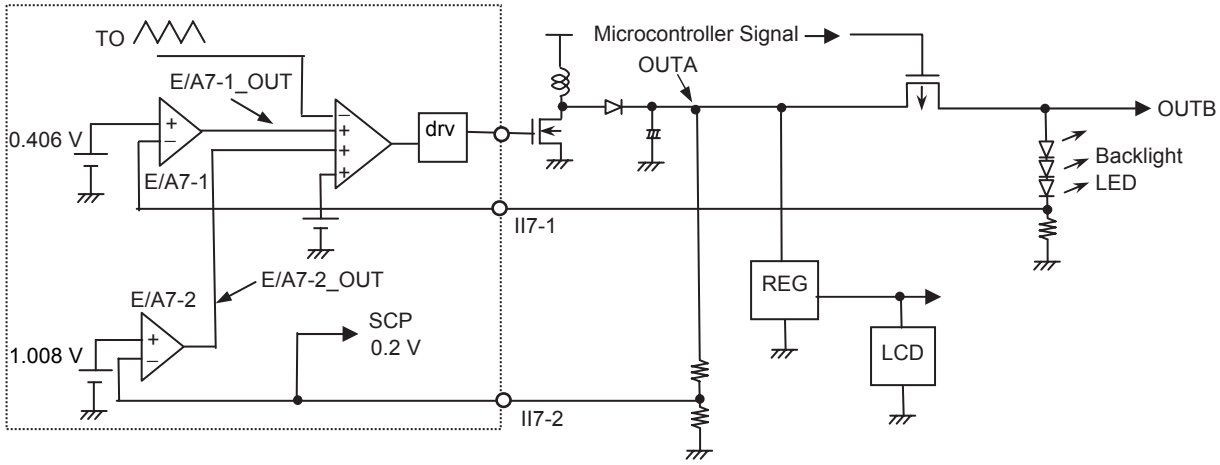
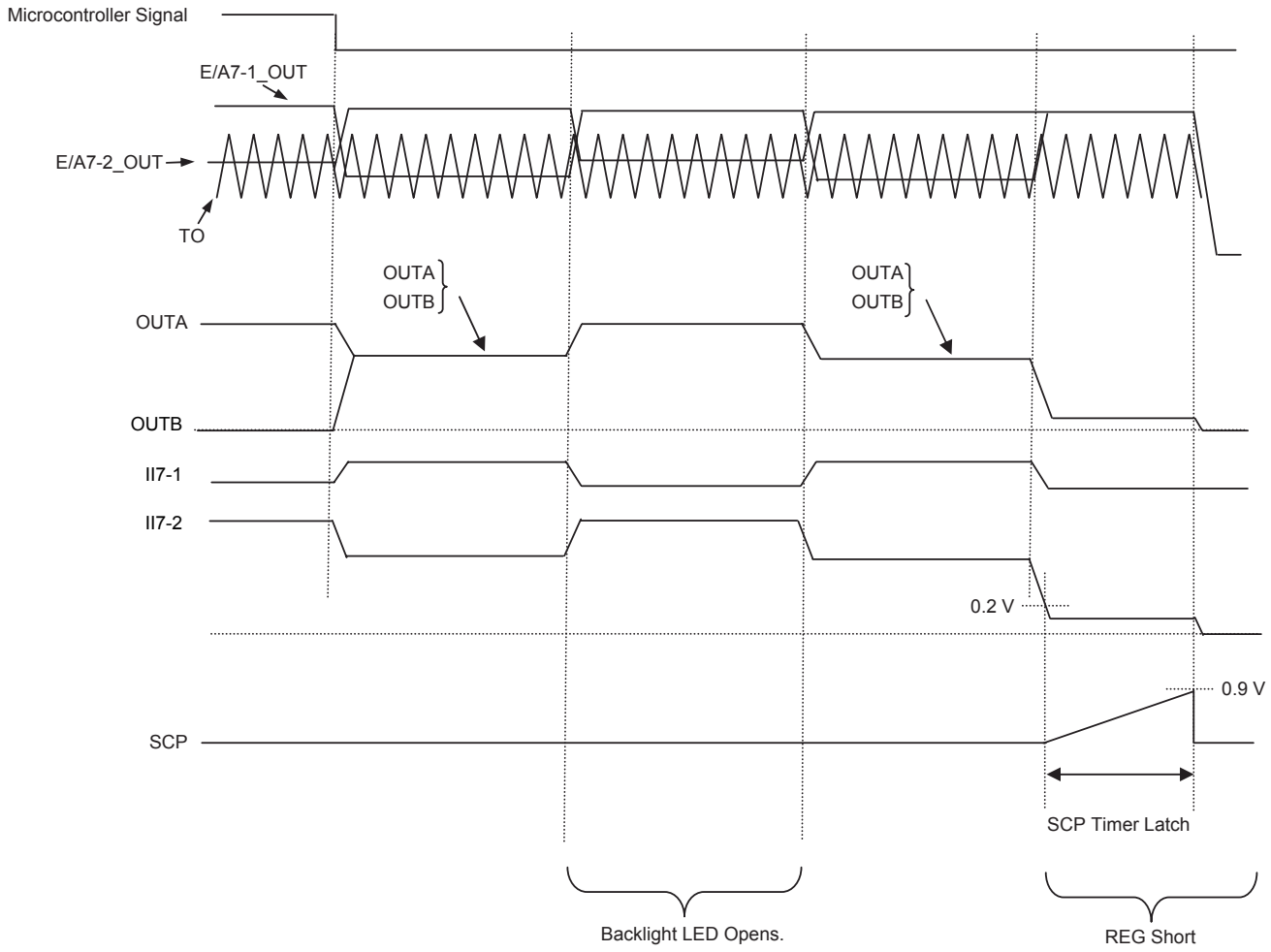


Figure 7-15



8. ADVICE ON DESIGNING

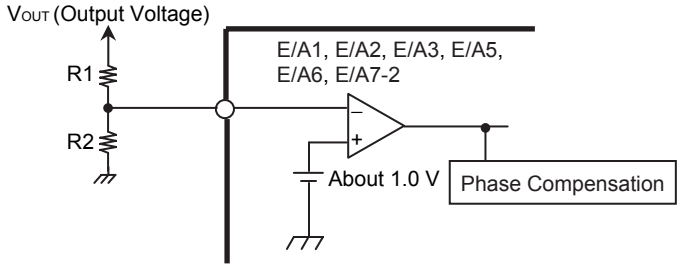
8.1 Setting Output Voltage

How to set the output voltage is illustrated below. The output voltage can be calculated by the expression below.

The input threshold voltages of the error amplifiers are about 1.0 V (TYP.) for E/A1, E/A2, E/A3, E/A5, E/A6, E/A7-2, and series regulator (ch8), 0.604 V (TYP.) for E/A4, and 0.406 V for E/A7-1 (TYP.).

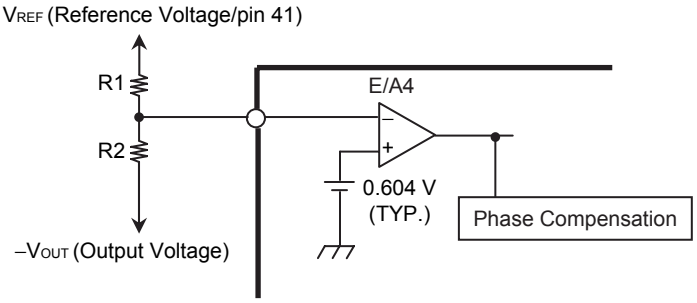
[Setting output voltage of ch1, ch2, ch3, ch5, ch6, ch7-2, ch8]

$V_{OUT} = (1+R1/R2) \times 1.0$



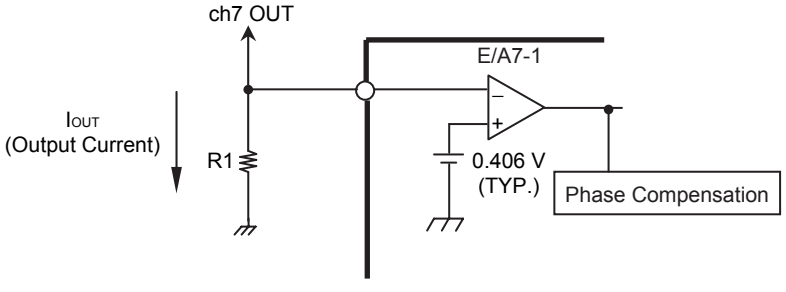
[Setting output voltage of ch4]

$V_{OUT} = V_{REF}-(V_{REF}-0.604) \times (R2+R1)/R1$



[Setting output current of ch7-1]

$I_{OUT} = 0.406/R1$



8.2 Setting Oscillation Frequency

The oscillation frequency can be arbitrarily set by the timing resistance connected to the RT pin (pin 48) and timing capacitance connected to the CT pin (pin 47).

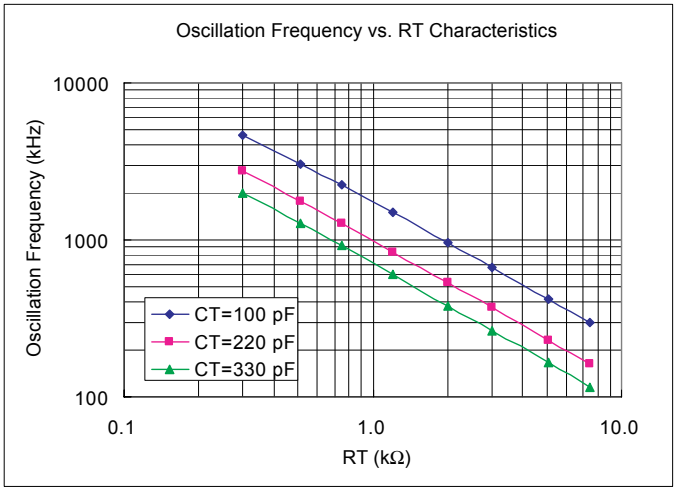
An approximate expression of the oscillation frequency (f_{OSC}) is shown below. However, because this expression is for approximation, mount the IC on the actual system and check the values of the parameters especially when the IC is used at a high frequency.

f_{OSC} = 0.2174/ (CT x RT) [Hz]
(Conditions: AV_{DD} = 5 V, T_A = 25°C)

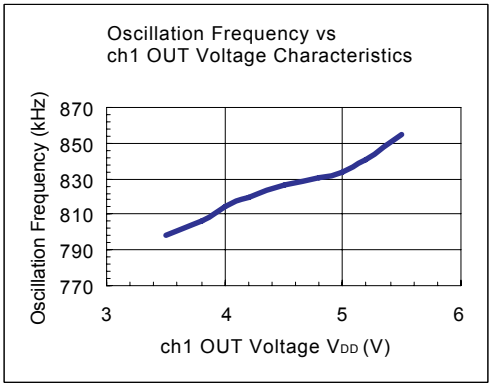
The oscillation frequency fluctuates depending on the voltage of the AV_{DD} pin (pin 34). An approximate expression including AV_{DD} is shown below. Again, mount the IC on the actual system and check the values of the parameters especially when the IC is used at a high frequency because this expression is for approximation.

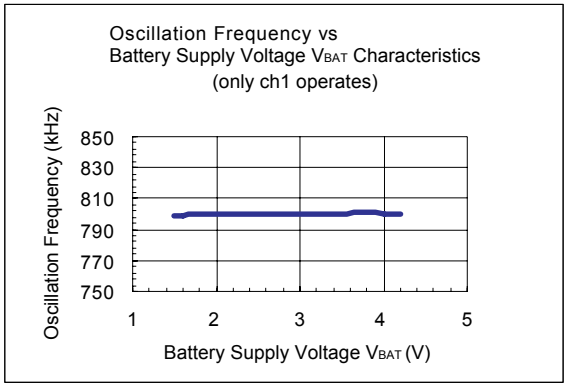
f_{OSC} = AV_{DD} x 27000 + 0.2174/ (CT x RT) – 135000 (Hz)
(Conditions: AV_{DD} = 3.5 to 5.5 V, CT = 220 pF, when about f = 800 kHz setup)

The following graph shows f_{OSC} vs. RT characteristics with CT as a parameter.



The frequency characteristics are as follows when the battery voltage fluctuates and when AV_{DD} fluctuates.





8.3 Calculating Delay Time of Short-circuit Protection Circuit

The following approximate expression is for calculating the delay time t_{DLY} of the short-circuit protection circuit.

t_{DLY} [s] = 1.059 x C_{SCP} [μF]

8.4 Pin Processing When Short-circuit Protection Circuit is not used

When the short-circuit protection circuit is not used, connect the SCP pin (pin 1) to the AGND pin (pin 46). At this time, closely monitor heating because the overheat protection circuit does not operate.

8.5 Preventing Malfunctioning of Short-circuit Protection Circuit

If noise is superimposed on the SCP pin (pin 1), the internal latch circuit may malfunction, stopping the output. To prevent this malfunctioning, prevent noise from being superimposed on the SCP pin by lowering the wiring impedance from the SCP pin to the AGND pin (pin 46).

If the delay time of the short-circuit protection circuit is set to be shorter than the internally fixed soft start time (4 ms (TYP.)), or if the load transient response of the DC-DC converter output is dull, the short-circuit protection may operate before the output voltage of a ch rises. Check the delay time of the short-circuit protection circuit by mounting the IC on an actual system.

9. NOTES ON USE

(1) Condition where protection circuits do not operate

The low-voltage malfunctioning prevention circuit is not connected to ch1. Also note that the short-circuit protection circuit and overheat protection circuit do not operate during the PFM operation.

When the SCP pin (pin 1) is connected to the AGND pin (pin 46), the overheat protection circuit does not operate.

(2) Pin connection

Be sure to apply the same potential to the power supply AV_{DD} pin (pin 34) and PV_{DD} pin (pin 17).

Supply a voltage so that (1ch output voltage = AV_{DD} pin voltage = PV_{DD} pin voltage) ≥ (VPIN2 pin voltage, VPIN3 pin voltage).

Connect all pins if there are two or more pins.

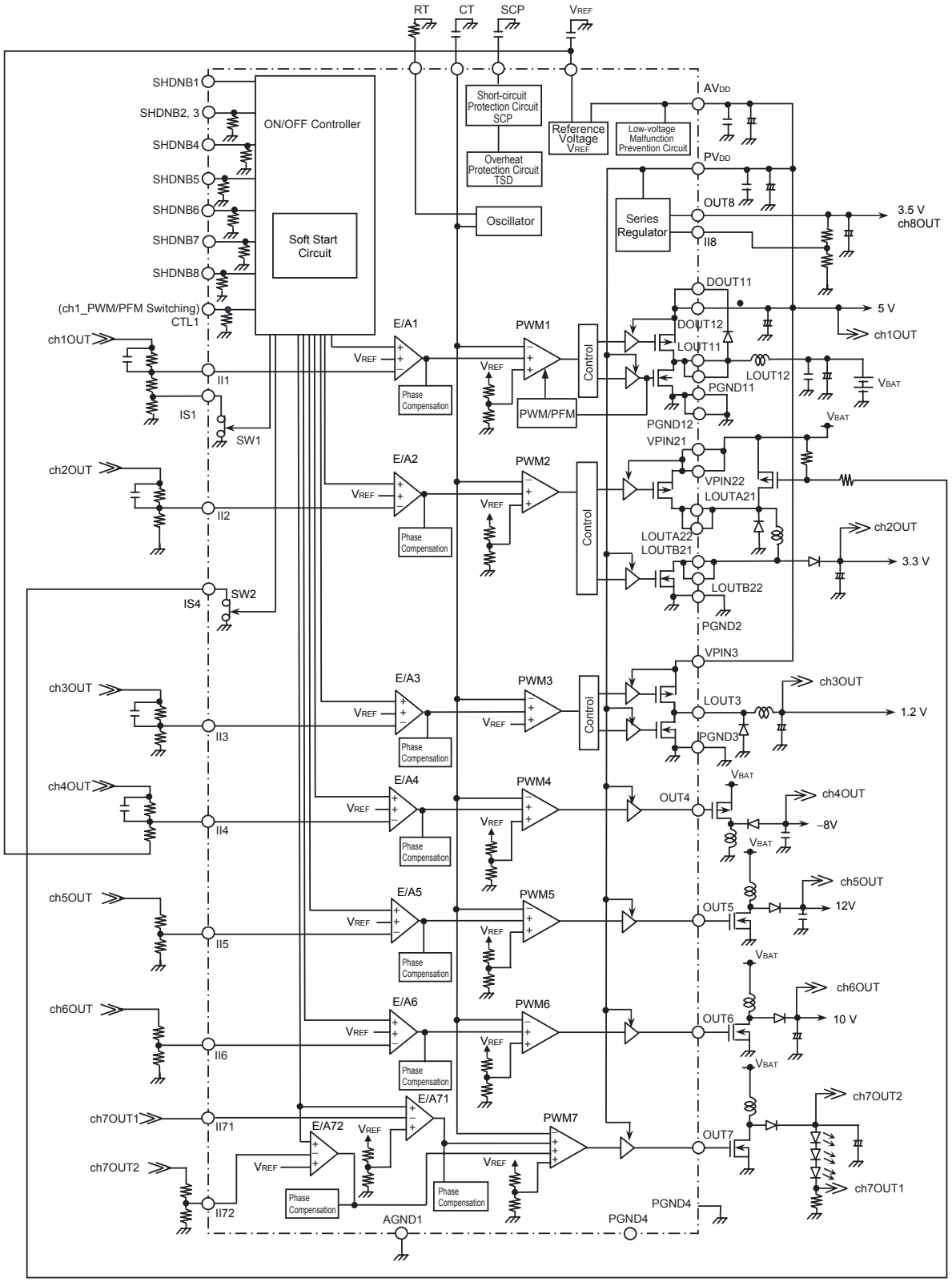
(3) Pull-down resistor of input pin

A pull-down resistor of 400 kΩ (TYP.) is connected to the input pin of the ON/OFF control block, but no pull-down resistor that suppresses the current consumption during the PFM operation of ch1 is not connected to SHDNB1 (pin 33).

(4) Actual pattern wiring

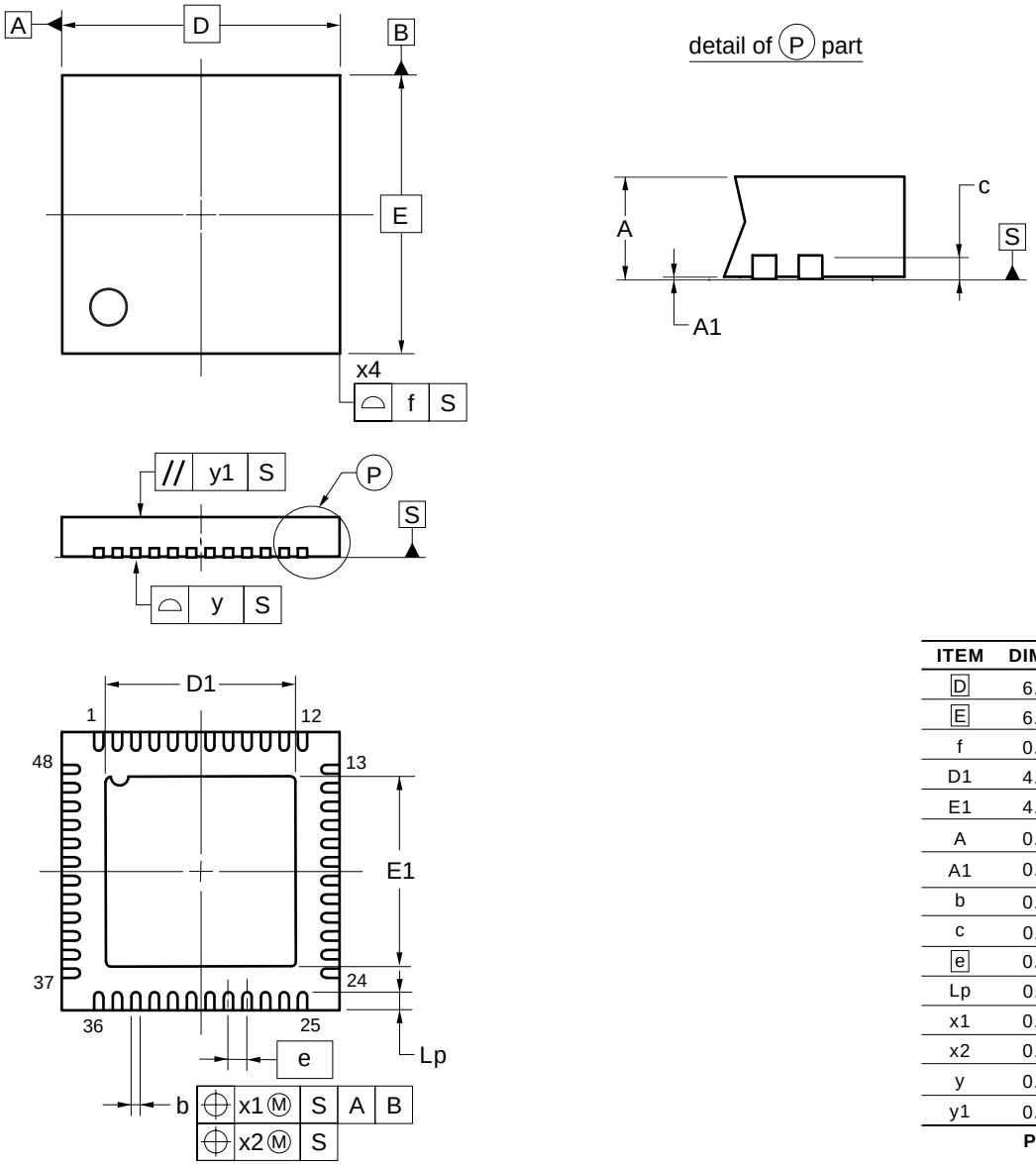
To actually perform pattern wiring, separate the ground of the control signals from the ground of the power signals, so that these signals do not have a common impedance as much as possible. In addition, lower the high-frequency impedance by using a capacitor, so that noise is not superimposed on the V_{REF} pin (pin 41).

10. APPLICATION CIRCUIT EXAMPLE



11. PACKAGE DRAWING

48-PIN PLASTIC VQFN (6x6)



(UNIT:mm)

ITEM	DIMENSIONS
D	6.00
E	6.00
f	0.10
D1	4.10±0.10
E1	4.10±0.10
A	0.85±0.05
A1	$0.02^{+0.03}_{-0.02}$
b	0.20±0.05
c	0.20
e	0.40
Lp	0.40±0.05
x1	0.10
x2	0.05
y	0.08
y1	0.10

P48K8-40-4E5

12. RECOMMENDED SOLDERING CONDITIONS

The μPD168802 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

μPD168802K8-4E5-E1-AT: 48-pin plastic VQFN

Soldering	Soldering Conditions	Recommended Method Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) Flux: Rosin flux with few chlorine (less than 0.2 Wt%)	IR60-107-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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