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| <p>Structure<br/>Product name<br/>Model No.<br/>Features</p> | <p>Silicon monolithic integrated circuit<br/>Strobe capacitor charging control IC<br/><b>BD4215NUV</b><br/>1. Built-in power transistor<br/>2. Adjustable transformer primary-side peak current to linear current with the I_PEAK pin<br/>3. Charging control switching with the CHARGE_ON pin<br/>4. Includes high precision full charge voltage detection circuit and output pin<br/>5. Various built-in protective circuits (TSD, UVLO, SDP)<br/>6. Built-in IGBT driver<br/>7. Employs small package: VSON010V3030 (3.0 mm × 3.0 mm × 1.0 mm)</p> |
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○ Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Rating	Unit
VCC supply voltage	VCC	-0.3 to 7	V
SW pin	Voltage	VSW	50
	Current *1	ISW	3
VOUT pin voltage	VVOUT	-14 to 50	V
Input pin voltage (CHARGE_ON, I_PEAK, FLASH_ON, IGBT_EN)	VI	-0.3 to 7	V
Operating temperature range	Topr	-20 to +85	°C
Storage temperature range	Tstg	-55 to +150	°C
Junction temperature	Tjmax	150	°C
Power dissipation	Pd	1270 <sup>*2</sup>	mW

○ Operating Conditions(Ta=25°C)

Parameter	Symbol	Rating	Unit
VCC supply voltage range	VCC	2.6 to 5.5	V
SW pin	Voltage	VSW	45
	Current *3	ISW	2.5
Input pin voltage (CHARGE_ON, I_PEAK, FLASH_ON, IGBT_EN)	VI	0 to VCC	V

\*1 Pulse width: 100 μs

\*2: Reduced by 10.16 mW/°C at Ta=25°C or more

(When mounted on a 74.2 mm×74.2 mm×1.6 mm glass epoxy, 4-layer board: Surface radiating copper foil of 6.28mm<sup>2</sup>, copper foil laminated in each layer)

○ Outside marking and dimension (UNIT:mm)

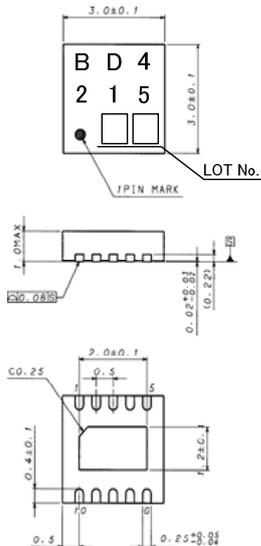


Fig.1 Outside marking and dimension

○ Pin No.

PIN No.	Pin Name	Function
1	PGND	Power GND pin
2	IGBT_OUT	IGBT Driver output pin
3	FLASH_ON	IGBT Driver output start signal input pin
4	XFULL	Full charge detection signal output pin
5	I_PEAK	Ipeak current control signal input pin
6	IGBT_EN	IGBT Driver operation restriction input pin
7	CHARGE_ON	Charge start signal input pin
8	VCC	VCC supply pin
9	VOUT	Secondary voltage detection pin
10	SW	Switching pin

Ⓢ This is not designed for radiation resistance.

Notes on this document

The Japanese version of this document is the formal specifications. The translated version of the document should be used for reference.

If there is any difference between the formal specifications and the translated version, the formal specifications shall take priority.

- Electrical Characteristics (Ta=25°C, VCC=V(CHARGE\_ON)=3.3V, V(L\_PEAK)=1.0V, V(FLASH\_ON)=0V, V(IGBT\_EN)=0V, unless otherwise specified.)

Parameter	Symbol	Target Value			Unit	Condition
		Min	Standard	Max.		
[Overall device]						
VCC current consumption 1	I <sub>CC1</sub>	65	90	145	mA	At Output ON, V(L_PEAK)=0V
VCC current consumption 2	I <sub>CC2</sub>	75	95	150	mA	At Output ON, V(L_PEAK)=1V
VCC current consumption 3	I <sub>CC3</sub>	115	140	200	mA	At Output ON, V(L_PEAK)=3V
Circuit current during standby operation	I <sub>STB</sub>	-	-	1	μA	V(CHARGE_ON)=0V
[Standby control CHARGE_ON pin]						
CHARGE_ON pin high voltage	V <sub>CH,H</sub>	2	-	-	V	
CHARGE_ON pin low voltage	V <sub>CH,L</sub>	-	-	0.6	V	
CHARGE_ON pin sink current	I <sub>(CHARGE_ON)</sub>	12	24	36	μA	V(CHARGE_ON)=3.3V
Unresponsive time when CHARGE_ON shorted	T <sub>(CHARGE_ON)</sub>	6	12.5	25	μs	
IC startup time	TOP	17.5	60	130	μs	Time for V(CHARGE_ON)="H"→VSW="L"
[Transformer primary-side driver block]						
SW pin leak peak current	I <sub>SWL</sub>	-	-	1	μA	V(SW)=45V
SW pin peak current 1	I <sub>PEAK1</sub>	0.77	0.87	0.97	A	V(L_PEAK)=0V
SW pin peak current 2	I <sub>PEAK2</sub>	1.57	1.67	1.77	A	V(L_PEAK)=3V
SW saturation voltage	V <sub>SAT</sub>	-	0.3	0.6	V	I(SW)=0.5A
[Charging characteristics adjustment block]						
L_PEAK sink current	I <sub>(L_PEAK)</sub>	-	2.5	5	μA	
Maximum ON time	T <sub>(ONMAX)</sub>	25	50	100	μs	
Maximum OFF time	T <sub>(OFFMAX)</sub>	12	25	50	μs	
[Transformer secondary-side detection block]						
Full charge detection voltage	V <sub>OUTTH</sub>	29.7	30	30.3	V	
Full charge detection voltage AC1	V <sub>OUTTH,AC1</sub>	29.66	30.27	30.87	V	Measured according to Fig. 2-1 Measurement Circuit Diagram.
XFULL reaction time	T <sub>(XFULL)</sub>	160	360	480	nsec	Measured according to Fig. 2-1 Measurement Circuit Diagram.
Full charge detection voltage AC2	V <sub>OUTTH,AC2</sub>	30.11	30.72	31.33	V	Measured according to Fig. 2-2 Measurement Circuit Diagram.
VOUT pin sink current	I <sub>(VOUT)</sub>	1	2	4	mA	V(VOUT)=30V
OFF detection voltage	V <sub>OFFL</sub>	-1.3	-0.5	-0.2	V	
XFULL pin high side ON resistance	R <sub>XFULLH</sub>	-	1	2	kΩ	V(XFULL)=VCC-0.5V
XFULL pin low side ON resistance	R <sub>XFULLL</sub>	-	1	2	kΩ	V(XFULL)=0.5V, V(VOUT)>VOUTTH
[Protective circuit block]						
UVLO detection voltage	V <sub>UVLOL</sub>	1.9	2.05	2.2	V	VCC detection (falling)
UVLO hysteresis width	V <sub>UVLOHYS</sub>	150	200	250	mV	
[IGBT driver block]						
High-level output short circuit current	I <sub>OSO</sub>	90	140	200	mA	V(FLASH_ON)=3.3V, V(IGBT_OUT)=0V, V(IGBT_EN)=3.3V, V(CHARGE_ON)=0V
Low-level output short circuit current	I <sub>OSI</sub>	25	40	55	mA	V(FLASH_ON)=0V, V(IGBT_OUT)=3.3V, V(IGBT_EN)=3.3V
FLASH_ON high-level input voltage range	V <sub>FLASH_ONH</sub>	2	-	-	V	V(IGBT_EN)=3.3V, V(CHARGE_ON)=0V
FLASH_ON low-level input voltage range	V <sub>FLASH_ONL</sub>	-	-	0.6	V	V(IGBT_EN)=3.3V, V(CHARGE_ON)=0V
FLASH_ON sink current	I <sub>(FLASH_ON)</sub>	12	24	36	μA	V(FLASH_ON)=3.3V
IGBT_EN high-level input voltage range	V <sub>IGBT_ENH</sub>	2	-	-	V	V(FLASH_ON)=3.3V, V(CHARGE_ON)=0V
IGBT_EN low-level input voltage range	V <sub>IGBT_ENL</sub>	-	-	0.6	V	V(FLASH_ON)=3.3V, V(CHARGE_ON)=0V
IGBT_EN sink current	I <sub>(IGBT_EN)</sub>	4.5	6.5	10	μA	V(IGBT_EN)=3.3V

- Measurement Circuit Diagram for Full Charge Detection Voltage AC1

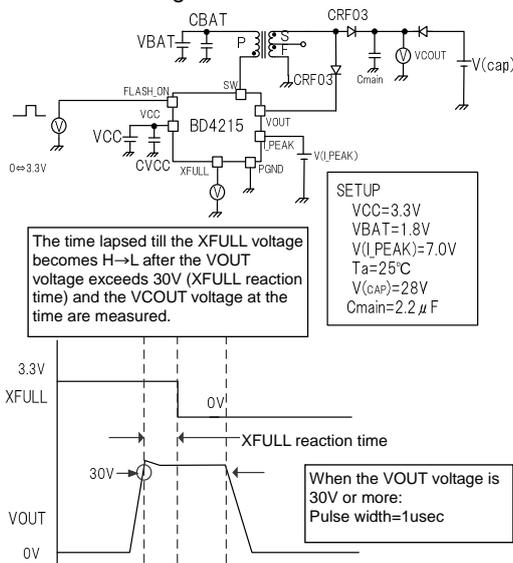


Fig.2-1 Measurement Circuit Diagram and Timing Chart

- Measurement Circuit Diagram for Full Charge Detection Voltage AC2

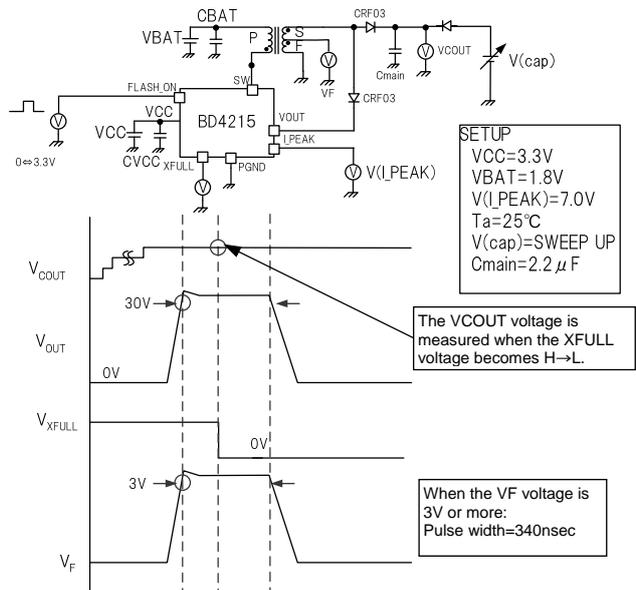


Fig.2-2 Measurement Circuit Diagram and Timing Chart

- Block Diagram

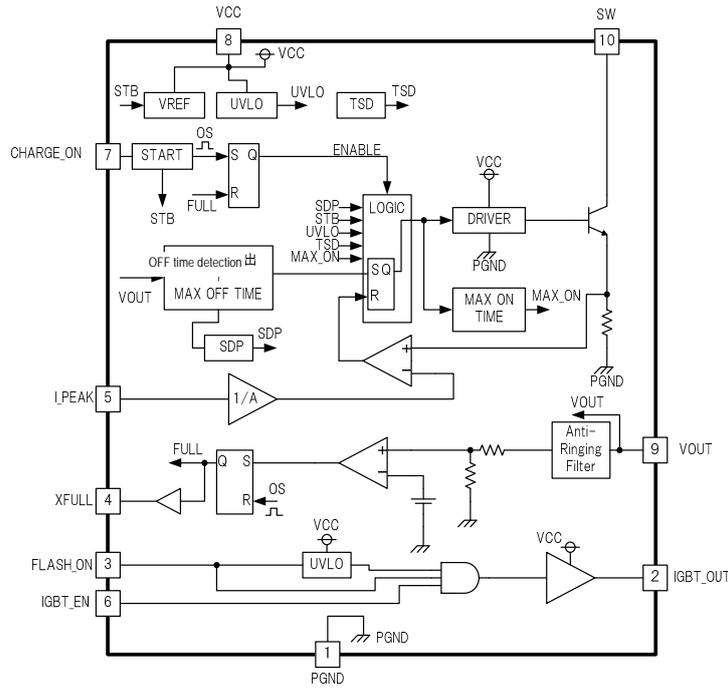


Fig.3. Block Diagram

○ UVLO, TSD and SDP

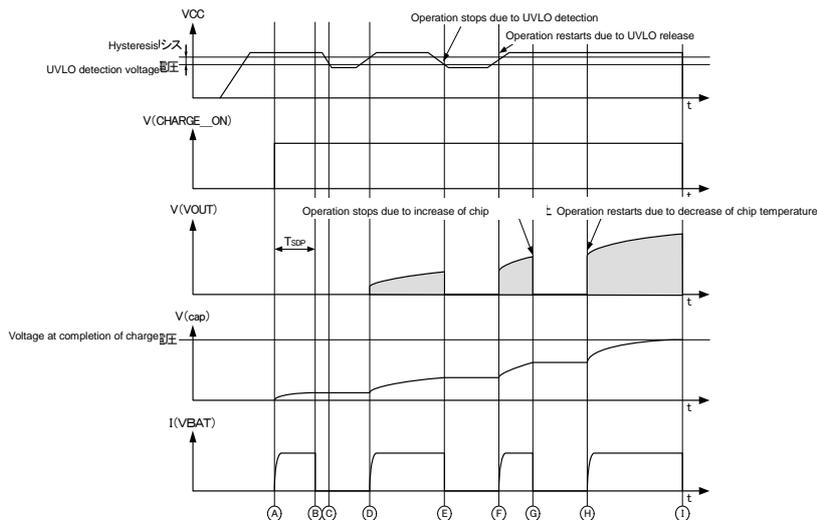


Fig.4 Timing Chart: Under Protective Circuit Operation

□ UVLO

If the VCC voltage is reduced to the UVLO detection voltage specified in the electrical characteristics or less, the UVLO protective circuit is activated and the charging operation temporarily stops. (See Time ㉓ and ㉔ in Fig.4.) After that, when the VCC voltage becomes the UVLO release voltage or more, the charging operation automatically restarts. (See Time ㉕ and ㉖ in Fig.4.)

This UVLO also works for the IGBT\_OUT pin. If the VCC voltage becomes the UVLO detection voltage or less, the IGBT\_OUT voltage is forced to be set to "L".

□ Thermal Shut Down (TSD)

It protects the IC against thermal runaway due to excessive temperature rise ( $T_j > 185^\circ\text{C}$ , [TYP]). After detection, the charging operation temporarily stops (See time ㉑ in Fig.4.), and when the chip temperature decreases, ( $T_j < 155^\circ\text{C}$ , [TYP]), it automatically restarts. (See Time ㉒ in Fig.4.)

□ VOUT pin short detection (SDP)

If the VOUT pin becomes the GND level due to any failure and the PowerTr repeats switching  $2^{16}$ (=65536) times which is the SDP count number (TSDP) at the maximum OFF time, it is judged as an error and the charging operation is forced to be stopped. (See Time ㉓ in Fig.4.) If the CHARGE\_ON pin is changed from "L" to "H" and the UVLO detection is released, it restarts.

○ **Precautions for Use**

1. **Absolute Maximum Rating**  
When impressed voltage, operating temperature range, etc., exceed the absolute maximum rating, the possibility of deterioration or destruction may exist. In addition, it is impossible to assume a destructive situation, such as short circuit mode, open circuit mode, etc. If a special mode exceeding the absolute maximum rating is assumed, please review to provide physical safety means such as fuse, etc.
2. **PGND potential (excluding SW, VOUT pins)**  
Maintain the PGND pin potential at the minimum level under the operating conditions. Furthermore, keep the pin except the PGND pin at a voltage higher than the PGND pin voltage including an actual transient phenomenon. However, keep the VOUT pin at a voltage higher than the voltage specified in the absolute maximum ratings.
3. **Thermal Design**  
Work out the thermal design with sufficient margin taking power dissipation (Pd) at the actual operation condition into account.
4. **Protective circuit**  
The output circuit of this IC does not have a built-in protective circuit against abnormal conditions such as overcurrent protection. Therefore, if a load exceeding the package power is applied or a short circuit occurs, the IC may be damaged. Before use, carefully design the circuit around the set.
5. **Short Circuit between Pins and Wrong Mounting**  
Sufficient caution is required for IC direction or displacement when installing IC on PCB. If IC is installed incorrectly, it may be broken. Also, the threat of destruction may exist in short circuits caused by foreign object invasion between outputs or output and GND of the power supply.
6. **Common Impedance**  
When providing a power supply and GND wirings, give sufficient consideration to lowering common impedance, reducing ripple (i.e. making thick and short wiring, reducing ripple by LC, etc.) as much as possible.
7. **IC Pin Input**  
This is the monolithic IC and has P<sup>+</sup> isolation and P substrate for element isolation between each element. By the P layer and N layer of each element, a P-N junction is formed and various parasitic elements are configured. For example, resistor and transistor are connected to a pin as shown in Fig.-5;
  - P-N junction operates as a parasitic diode when GND > (Pin A) in the case of the resistor, and when GND > (Pin B) in the case of the transistor (NPN).
  - Also, a parasitic NPN transistor operates by the N layer of another element adjacent to the previous diode in the case of a transistor (NPN) when GND > (Pin B).
 The parasitic element consequently emerges through the potential relationship because of IC's structure. The parasitic element pulls interference out of the circuit which may be the cause of malfunction or destruction. Therefore, excessive caution is required to avoid operation of the parasitic element which is caused by applying voltage to the input pin lower than GND (P board), etc.

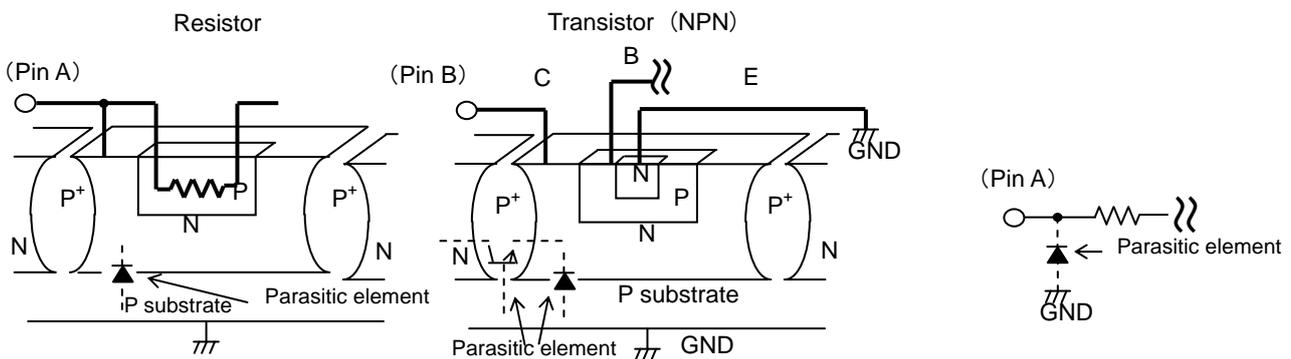


Fig.5 Simplified Structure Example, Bipolar IC

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