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ROHM

STRUCTURE PRODUCT SERIES Silicon Monolithic Integrated Circuit

7-Channel Switching Regulator Controller for Digital Camera

TYPE BD9740KN

FEATURES

Wide input voltage range (1.5V to 10V)

 controls up to 7 switching regulators: Step up converter(1channel), Step-down converter(1channel), Configurable for step-up or step-down conversion(3channels), Positive to negative converter(1channel), Step-up converter for LED (1channel)

Synchronous rectifying action mode (2channels) Built-in FET Transistor (1channel)

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	units	
Power Supply Voltage	VBAT VCC,PVCC	-0.3~12	V	
	PVCCH	-0.3~15	V	
Power Input Voltage	DRAIN4H,4L	-0.3~12	V	
	OUT1B	-0.3~20	V	
Power Dissipation	Pd	500(*1)	mW	
Tower Dissipation	Tu	760(*2)	mW	
Operating Temperature	Topr	-25~+85	°C	
Storage Temperature	Tstg	−55~+125	°C	

(*1)Without external heat sink ,the power dissipation reduces by 5.0mW/°C over25°C. (*2)Reduced by 7.6mW/°C over25°C, when mounted on a PCB(70.0mm × 70.0mm, 1.6mm)

ORecommended operating conditions

Parameter	symbol					
raiai lietei	Symbol	Min.	Тур.	Max.	units	
	VBAT	1.5	-	10	٧	
Power Supply Voltage	VCC,PVCC	2.5	_	10	٧	
	PVCCH	4.0		14	٧	
VREF Pin Connect Capacitor	CVREF	1.0	-	4.7	μF	
VREGA Pin Connect Capacitor	CVREGA	1.0	_	10	μF	
SCP Pin Connect Capacitor	CSCP	0.001	-	2.2	μF	
SS1 Pin Connect Capacitor	CSS1	0.001	_	2.2	μF	
[Oscillator]						
Oscillator Frequency	fosc	0.1	_	1,2	MHz	
OSC Timing Resistor	нт	4.7	_	30	kΩ	
OSC Timing Capacitor	СТ	100	_	10000	ρF	

Parameter	symbol		Standard valu	Units	
		Min.	Тур.	Max	1
[Driver]					
DRAIN Pin Input Voltage	VDRAIN	_		10	V
Non FET Output Current (CH4)	loFET4	_	_	700	mA
Driver Output Current (CH1~3, 5~7)	lout	_	-	30	mA
Driver Peak Current (CH1~3, 5~7)	lpeak	-	-	200	mA
Built-in NPN TR Sink Current(CH1)	INPNsink		_	500	mA

(*3) VREGA drops under VCC=2.8V

It is strongly recommended that a capacitor be connected to VREF and VREGA pin to prevent oscillation.

The IC may not operate properly due to undetermined state of the internal logic when Vcc voltage is applied suddenly while STB pins are already ON.
In this case make sure STB pins are initially OFF.



○Absolute maximum ratings(Ta=25°C)

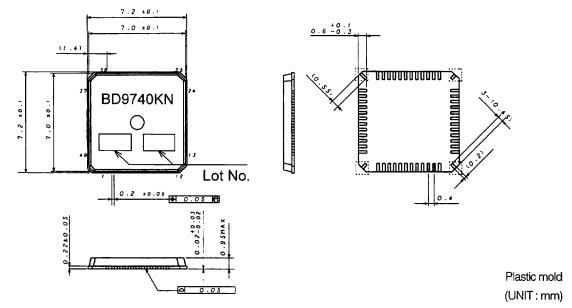
			Spec.	-	T	
Parameter	Symbol	Min.	Тур.	Max	Units	Conditions
[Reference Voltage]				r		
Reference Voltage	Vref2	0.99	1.0	1.01	٧	
Line Regulation	DVLi	-	4.0	125	m∨	Voc=3.0V ~9.0V
Load Regulation	DVLo	-	1.0	7.5	mV	Iref=10 μA ~100 μA
Short-Circuit Output Current	los	02	1	-	mA.	Vref=0V
[Internal Regulator]	LECOA		- 65			
REGA Output Voltage Low Voltage Input Prever	VREGA nted Operation	2.4 Faults Circu	2.5 t)	2.6	į v	lreg=5mA
Threshold Voltage 1	Vstd1	3.45	3.6	3.75	V	PVCCH monitor
Hysteresis width 1	∆Vst1	_	300	_	mV	
Threshold Voltage 2	Vstd2	2.3	2.4	2.5	V	VCC monitor
Hysteresis width 2	ΔVst2	_	200		mV	
Threshold Voltage 3	Vstd3	-	2.0	-	V	VREGA monitor
Hysteresis width 3 (Start up Circuit)	ΔVst3	_	50		m∨	
Oscillator Frequency	Fstart	50	120	220	kHz	
Minimum VBAT Voltage	Vst1	1.5	-	-	v	
Slow Sart Charge Current	lss1	1.1	22	3.3	μА	Vss=0V
[Protection Circuit] Timer Start Threshold Voltage	Vtc	21	22	23	V	FB monitor
SCP Output Current	Isop	2	4	6	μА	VSCP=0.1V
SCP Threshold Voltage	Visc	0.9	1.0	1.1	٧	
SCP Standby Voltage [Triangular wave oscillator	Vssc	_	22	170	mV	
Oscillator Frequency	fosc1	450	500	550	KHz	RT=11kohm, CT=180pF
Frequency Stability (Vcc)	Df	-	0.3	2	%	VCC=3.0V~9.0V
RT Output Voltage	VAT	0.78	1.00	1.22	٧	
[Error Amp 1 ~4] Low-level Output Voltage	VOL	г	1.3	r <u>-</u>	l v	INV=2V
High-level Output Voltage	VOH	VREGA	-	_	v	INV=0.5V
Meximum Sink Current	IOI	-0.3V 36	72		μА	FB=1.7V,
Maximum Source Current	100	36	72	-	μА	VINV=1,1V FB=1.7V, VINV=0.9V
[EnorAmp 5]						
Low-level Output Voltage High level Output	VOH	VREGA	1.3	- -	V	INV=2V
Voltage Maximum Sink Current		-0.3	70	<u> </u>	 	INV=0.5V FB=1.7V,
Maximum Source	100	36	72	 -	μΑ	VINV=1,1V FB=1.7V,
Current DTC resistance VREGA		36	72	-	μA	VINV=0.9V
side DTC resistance GND	RDTCU5 RDTCD5	20 65	96 96	40 125	ΚΩ	
side [(Error Amp6)	TIDIOLO	L	30	123	I NV	
Low-level Output Voltage	VOL		1.3	I	V	NON6=-0.2V
High-level Output Voltage	VOH	VREGA 0.3	_		v	NON6=0.5V
Maximum Sink Current	Ю	36	72	_	μА	FB6=1.7V NON6=-0.2V
Low-level Output Voltage	100	36	72		μΑ	FB6=1.7V NON6=0.5V
DTC resistance VREGA side	RDTCU6	20	30	40	kΩ	
DTC resistance GND side	RDTCD6	65	96	125	kΩ	
NON6 input range	VRES6	-0.3	-	1.5	V	

Paramet	er	Symbol	L.,	Spec.		Units	Conditions
(Error Amp			Min.	Тур.	Max		
Low -level Cuty		- VOL		1.3	_	v	INV=2V,
High -level Output Voltage		VOH	VREGA	_	_	v	NON7=1V INV=0.5V,
Maximum		IOI.	-0.3 36	72		μА	NON7=1V FB7=1.7V,
Sink Currer Waximum Sou		100	36	72		μА	INV7=0.5V FB7=1.7V,
NON7 inpu		VRES7	0		1.5	V	INV7=1.5V
DTC resistance		RDTCU	20	30	40	kΩ	
DTC resistance	GND side	RDTCD	65	95	125	kΩ	
[PWM Con	noarator 1	7					
	hreshold	Vto	-	1.49		V	V1:DUTY0%
Voltage		Vt100	_	1.95		v	V1:DUTY100%
MAX DUTY (step-down)	(1,2,3	Dmax1	_	100	_	%	UDSEL=VCC
	JTY1,2,3	Dmax3	77	85	93	%	UDSEL=0V
MAX DUTY4		Dmax2	_	100		%	
MAX DUTYS	,6,7	Dmax4	77	85	93	%	
[Output circ							
High-level Voltage on D	Output riving	VSATH	VCC -1.6	VC -0.8	_	V	lo=30mA, CH1~3,5~7
Low-level Voltage on D	Output riving	VSATL	_	0.8	1.6	٧	lo⇒30mA
Hi-side Nich Resistor	FET ON	RoniH4	-	300	500	mΩ	PVCCHL5V
Lo-side Noh Resistor	FETON	RonL4	-	300	500	mΩ	PVCCH-5V
(Step-up/do	wn Selecto	r)					
UDSEL123 Control	Step down	VUDDO	VCC ×0.7	•	vcc	٧	
Voltage	Step	VUDUP	0		VCC ×0.3	٧	
Soft-Start							
Soft-start time	CH4	Tss1	1.8	3.6	6.0	msec	VCC=PVCC=5V PVCCH=5.0V STB 0→3V
Soft-start time	CH2,CH3	Tss2	1.8	3.6	6.0	msec	VCC=PVCC=5V STB=3V INV4=0→1.2V
INV4 voltage CH2,3	to start	VPG4	0.72	0.80	0.88	٧	VCC=PVCC=5V PVCCH=5.0V
[STB1~7]	L 01:	HOTOLIC					
STB Control	ON	VSTBH1	2.0		11	<u> </u>	
Voltage1	OFF	VSTBL1	-0.3	-	0.3	l v	
STB Pull-dow	n Resistor	RSTB1	250	400	700	ΚΩ	
[Circuit Cur							
Stand by Current1 (VBAT sink current)		ISTB1	-	-	5	μΑ	STB1~7=0V
Sand by Current2 (VCC, PVCC sink current)		ISTB2	-		5	μΑ	STB1~7≡0V
Start up Current (VBAT sink current)		IST		30	100	mA	CT=1.7V VCC=0V
Oircuit Current on Driving1 (VBAT sink current)		loc1	-	100	300	μА	CT=1.7V
Circuit Current on Driving2 (VCC,PVCC sink current)		loc2		5	15	mA	CT=1.7V INV=2.5V

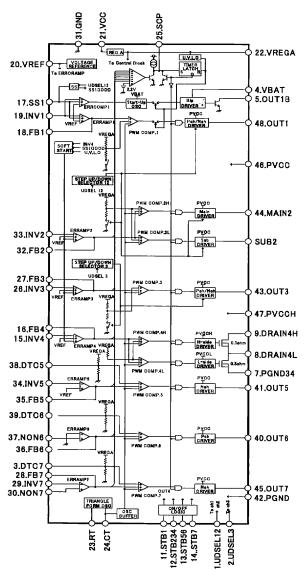
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PACKAGE



OBlock diagram



Pin No.	Pin Name		
4	VBAT		
21	VCC		
46	PVCC		
10	PVCCH		
42	PGND		
6,7	PGND4		
31	GND		
22	VREGA		
40,41,45,47,48	OUT1,3,5,6,7		
44	MAIN2		
43	SUB2		
5	OUT1B		
9	DRAIN4H		
8	DRAIN4L		
20	VREF		
3,38,39	DTC 5~7		
16,18,27,28,32,35,36	FB 1~7		
15,19,26,29,33,34	INV 1~5,7		
30,37	NON6,NON7		
17	SS1		
23	RT		
24	CT		
25	SCP		
1	UDSEL12		
2	UDSEL3		
11,12,13,14	STB1,234,56,7		



ONOTE FOR USE

Absolute maximum rating

The device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the source, such as short mode or open mode, cannot be identified if the device is destroyed, it is important to take physical safety measures (such as fusing) if a special mode in excess of absolute rating limits is to be implemented.

(2) Supply line

Since the motor's reverse electromotive force gives rise to the return of regenerative current, measures should be taken to establish a channel for the current, such as adding a capacitor between the power supply and GND. In determining the approach to take, make sure that no problems will be posed by the various characteristics involved, such as capacitance loss at low temperatures with an electrolytic capacitor.

(3) GND potential

Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.

(4) Thermal design

Be sure to factor in allowable power dissipation (Pd) in actual operation, and to build sufficient margin into the thermal design to accommodate this power loss.

(5) Operation in strong magnetic fields

Use in strong electromagnetic fields may cause malfunctions. Exercise caution with respect to electromagnetic fields.

(6) ASO

Set the parameters so that output Tr will not exceed the absolute maximum rating or ASO value when the IC is used.

(7) Thermal shutdown circuit

This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the chip temperature reaches the threshold value listed below. When TSD is on, the device goes to high impedance mode. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

(8) Mutual impedance

Use short and wide wiring tracks for the main supply and ground to keep the mutual impedance as small as possible. Use inductor and capacitor network to keep the ripple voltage minimum.

(9) Voltage of STB pin

The threshold voltages of STB pin are 0.3V and 2.0V. STB state is set below 0.3V while action state is set beyond 2.0V. The region between 0.3V and 2.0V is not recommended and may cause improper operation.

(10) Setting Max Duty

Max duty limit might not work normally at high frequency. Consider adequate margin when operating circuit above the maximum allowable switching frequency.

(11) Please use the same power supply of driver block as that of main block.

This IC can't be used on the application that arbitrary voltage is applied to driver block.

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