STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT SERIES Strobe Charge Control IC

TYPE **BD4225NUX**

Functions
1. Built-in Low Vth DMOS 45V
2. Adjustable transformer primary-side peak current by RADJ pin
3. Standby mode switching with the START pin.
4. Includes charge complete signal output (FULL) pin.
   Includes charge voltage detection (VC) pin (can be set externally).
5. Built-in thermal shutdown circuit (TSD).
   Built-in under voltage looked out (UVLO).
6. Built-in transformer secondary-side OPEN, SHORT protection.
7. SON 10pin package VSONO10X3020(3.0mm×2.0mm×0.6mm)

○ Absolute maximum ratings(Ta=25℃)

Parameter	Symbol	Limit	Unit
VCC pin	VCC	−0.3 to 7	V
SW pin	VSW	45	V
VC pin	VC	−0.3 to 7	V
START pin	START	−0.3 to 7	V
FULL pin	FULL	−0.3 to 7	V
IGBT_IN pin	IGBT_IN	−0.3 to 7	V
Operating temperature	Topr	−35 to 85	℃
Storage temperature range	Tstg	−55 to 150	℃
Junction temperature	Tjmax	150	℃
Power dissipation	Pd	1540	mW

Reduced by 12.32 mW/° C over Ta = 25° C. (When mounted on 74.2 mm × 74.2 mm × 1.6 mm, glass epoxy)

○ Recommended operating ranges

Parameter	Symbol	Limit	Unit
VCC power supply input voltage range	VCC	2.5 to 5.5	V
VC pin input voltage range	VC	-0.3 to VCC	V
START pin input voltage range	VSTART	0 to VCC	V
IGBT_IN pin input voltage range	VIGBT_IN	0 to VCC	V
FULL pin input voltage range	VFULL	0 to 5.5	V
SW pin current	ISW	0 to 2	A

○ Electrical characteristics (Ta=25℃, VCC=V(START)=3.3 V, V(IGBT_IN)=0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Overall device]						
VCC circuit current	ICC	—	1.5	3	mA	
Circuit current standby operation	ISTB	—	—	1	μA	START=0V
[Standby control START pin]						
START pin high voltage H1	VSTH1	1.7	—	—	V	
START pin high voltage H2	VSTH2	1.5	—	—	V	Ta=-25℃～85℃,VCC=2.5V～5.0V
START pin low voltage	VSTL	—	—	0.6	V	
Input bias current	ISTART	14	28	42	μA	START=3.3V
[Transformer primary-side driver block]						
SW pin leak current	ISWL	—	—	1	μA	SW=45V
SW pin peak current	IPEAK	0.4	0.5	0.6	A	RADJ=100kΩ
SW saturation voltage	VSAT	—	0.2	0.4	V	ISW=0.5A
RADJ adjustable range	RADJ	33	—	100	kΩ	
[Charging control block]						
Max on time	TONMAX	20	40	100	μs	
Max off time	TOFFMAX	10	20	50	μs	
[Transformer secondary-side detection block]						
VC pin input current	IVC	—	—	1	μA	VC=VCC
Full charge detection voltage	VFULLTH	0.989	1	1.011	V	
Full charge detection voltage AC1	VFULLTH_AC1	0.9890	1	1.0135	V	VC=200ns pulse input→FULL=H→L
Full charge detection voltage AC2	VFULLTH_AC2	0.9890	1	1.0160	V	VC=100ns pulse input→FULL=H→L
FULL pin ON resistor	RFULLL	0.5	1	2	kΩ	VC=VCC,FULL=0.5V
FULL pin leak current	IFULLL	—	—	1	μA	FULL=3.3V
[Protection circuit block]						
UVLO detect voltage	VUVLOTH	1.95	2.1	2.25	V	VCC detection
UVLO hysteresis	VUVLOHYS	120	200	280	mV	
[IGBT driver block]						
Output short high current	Ioso	90	140	200	mA	IGBT_IN=3.3V,START=0V,IGBT_OUT=0V
Output short low current	Iosi	15	30	60	mA	IGBT_IN=0, START=0V,IGBT_OUT=3.3V
IGBT_IN input high voltage range H1	VIGBTH1	1.7	—	—	V	START=0V
IGBT_IN input high voltage range H2	VIGBTH2	1.5	—	—	V	START=0V, Ta=-25℃～85℃,VCC=2.5V～5.0V
IGBT_IN input high voltage range	VIGBTL	—	—	0.6	V	START=0V
IGBT_IN sink current	IIGBT_IN	12	24	36	μA	START=0V
IGBT_IN response time Rise	Tres_rise1	—	1	2	μs	IGBT_IN→IGBT_OUT response time(rise)
IGBT_IN response time Fall	Tres_fall1	—	120	200	ns	IGBT_IN→IGBT_OUT response time(fall)
IGBT_IN response time Rise	Tres_rise2	—	15	80	ns	IGBT_IN→IGBT_OUT response time(rise)
IGBT_IN response time Fall	Tres_fall2	—	120	200	ns	IGBT_IN→IGBT_OUT response time(fall)

◎This product is not designed for normal operation within a radioactive environment

○ Block Diagram

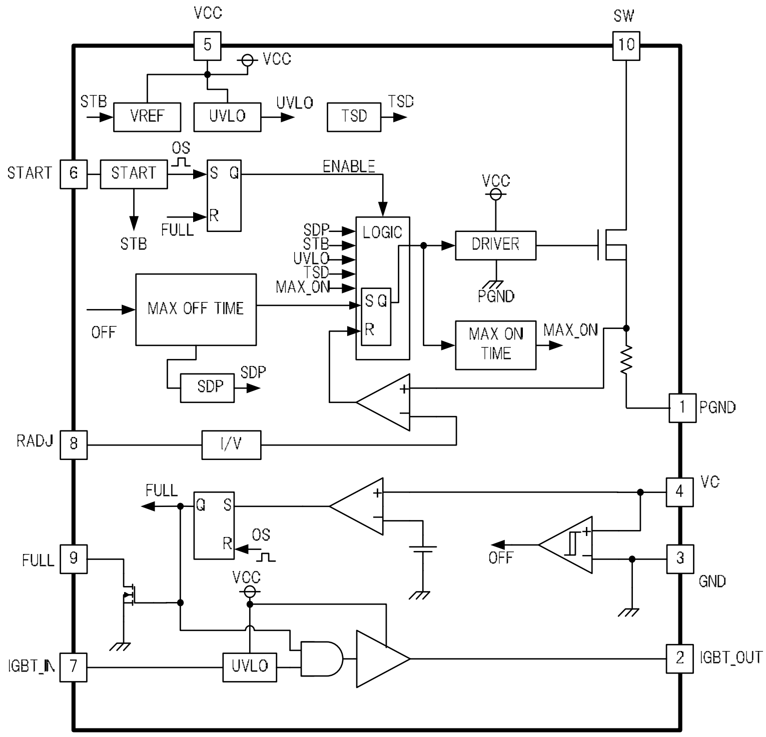
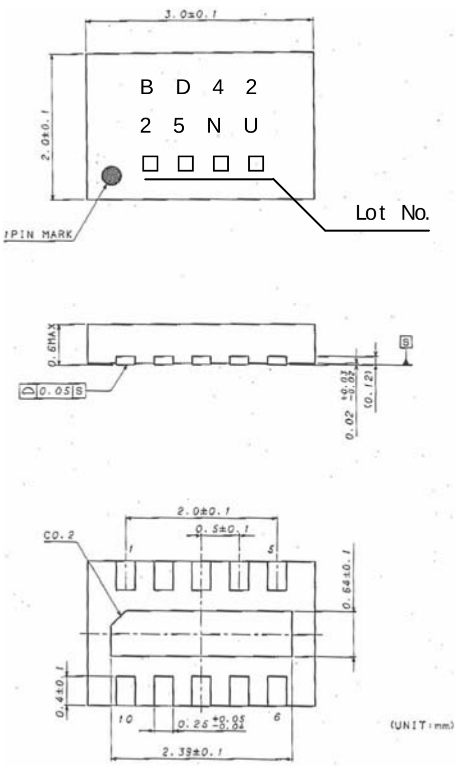


Fig.1 Block Diagram

○Package (UNIT:mm)



○ Pin No.

Pin No.	Pin Name	Function
1	PGND	Power GND
2	IGBT_OUT	IGBT driver output
3	GND	Ground pin
4	VC	Secondary-side voltage detection pin
5	VCC	VCC supply pin
6	START	Standby pin
7	IGBT_IN	nput terminal of trigger signal for starting output of IGBT driver
8	RADJ	primary-side current control pin
9	FULL	FULL charge detection flag pin
10	SW	Switching pin

○ Cautions on use

1. Absolute maximum ratings

   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. GND and PGND potential

   Ensure a minimum GND and PGND(Except for SW pin and VC pin) pin potential in all operating conditions. In addition, ensure that no pins other than the GND and PGND pin carry a voltage less than or equal to the GND and PGND pin, including during actual transient phenomena.

   Don't use VC pin under Absolute Maximum Rating.

3. Thermal design

   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4. Protect circuit

   The IC does not incorporate built-in malfunction protection such as overcurrent protection, short detection, or thermal shutdown circuitry. For this reason, the IC may be damaged if it is shorted or subjected to a load that exceeds the package power. The design of peripheral application circuits should reflect these potential risks.

5. Inter-pin shorts and mounting errors

   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

6. Common impedance

   The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

7. IC Pin Input

   This is the monolithic IC and has P^+ isolation and P substrate for element isolation between each element. By the P layer and N layer of each element, a P-N junction is formed and various parasitic elements are configured.

   For example, in the case of a resistor and transistor being connected to a pin as shown in Fig.-3;

   P-N junction operates as a parasitic diode when GND > (Pin A) in the case of the resistor, and when GND > (Pin B) in the case of the transistor (NPN)

   Also, a parasitic NPN transistor operates by the N layer of another element adjacent to the previous diode in the case of a transistor (NPN) when GND > (Pin B).

   The parasitic element consequently emerges through the potential relationship because of IC's structure. The parasitic element pulls interference out of the circuit which may be the cause of malfunction or destruction. Therefore, excessive caution is required to avoid operation of the parasitic element which is caused by applying voltage to an input pin lower than GND (P board), etc.

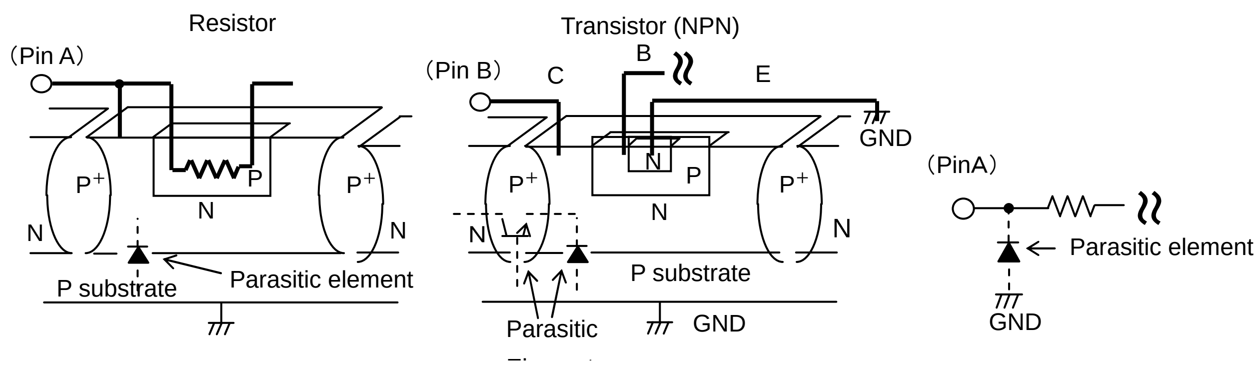


Fig.3 Other adjacent elements

Notes

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